

RogueOne 13" Schematics

Whiskey Lake-U

2018-07-09

REV : A00 (17925-1)

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DY : None Installed
UMA: UMA only installed

<Core Design>



Wistron Corporation
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Title

Cover Page

Size
A3

Document Number

RogueOne 13"

Rev

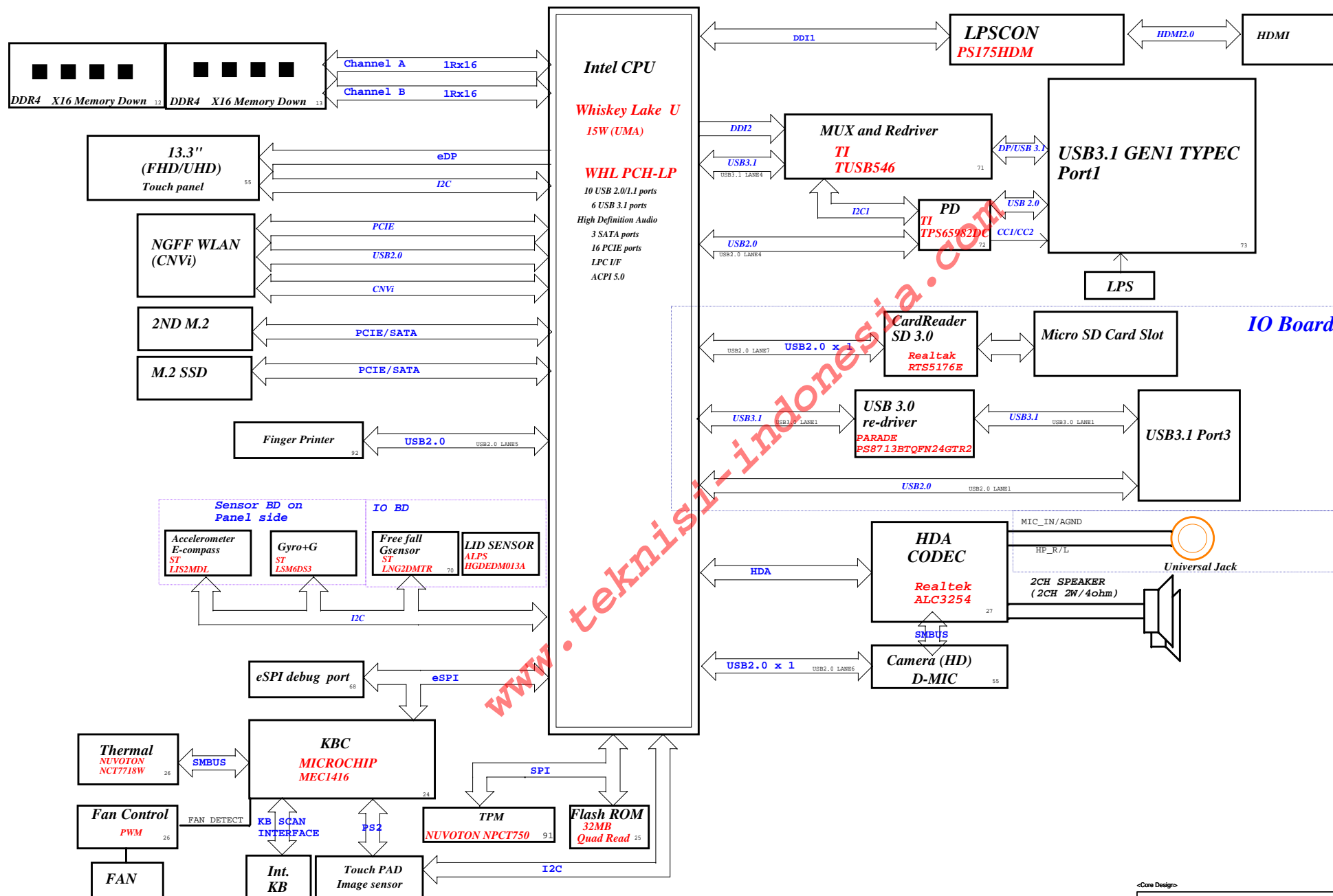
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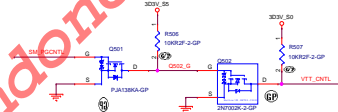
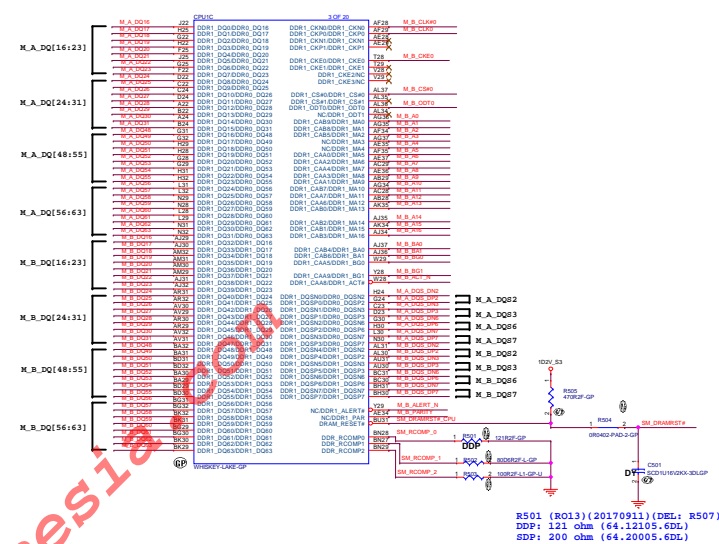
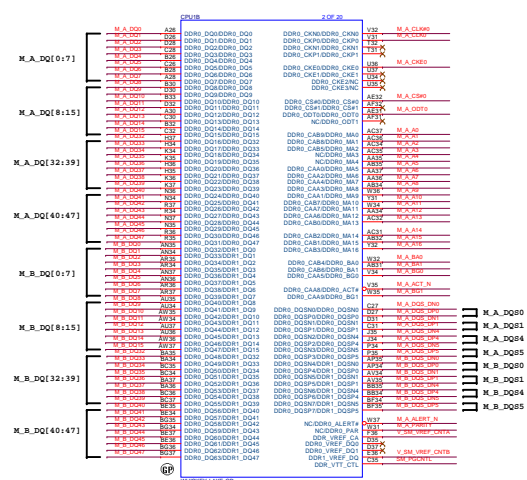
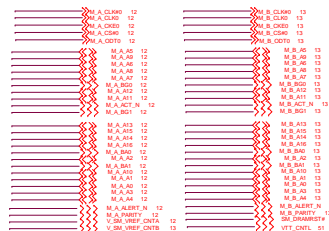
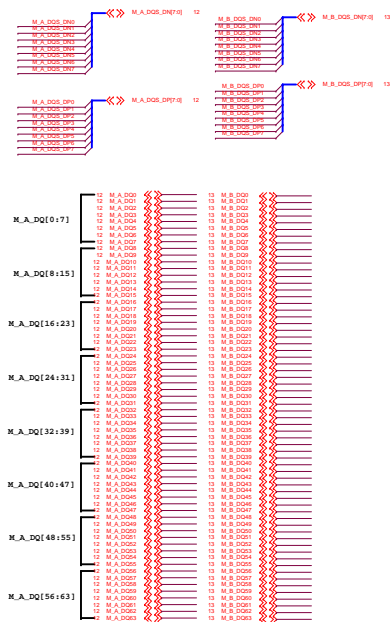
Date: Thursday, August 02, 2018

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WHL-U 13" CPU 15W Block Diagram

Project code: 4PD0EZ010001
PCB P/N: 17925
Revision: -1





SM_RCOMP keep routing length less than 500 mils

Table 4-8. WHL U DDR4 x16 Memory Down Routing Guideline (mils)

RCOMP (0/1/2)	M	US/SL	500				10	10	20								CPL-143e; WHLU42; {0} 121/2000 {1} 66.6 {2} 160 CML-U22; {0} 160 {1} 100 {2} 100
				CPL-143e/WHLU42; RCOMP[0] value for SDP = 200+/-1% ohm, and for DOP is 121 +/- 1% ohm CML-U22; all RCOMP values 100 Ohm													
RCOMP values																	

PDG: DDR/ODT

4.3 ODT Connectivity

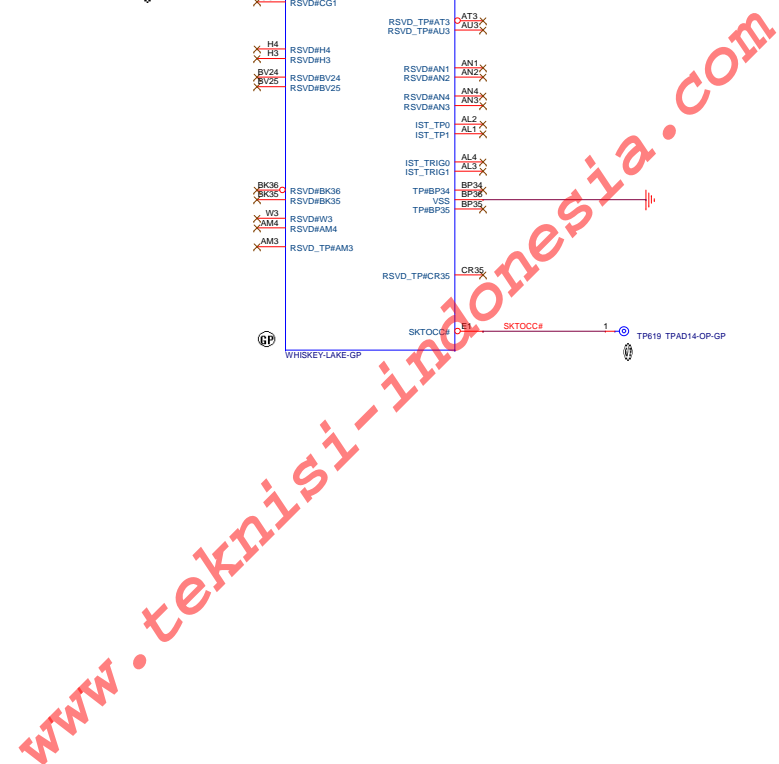
Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	DDR4 SODIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

Note:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

Note:

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.



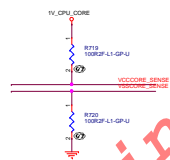
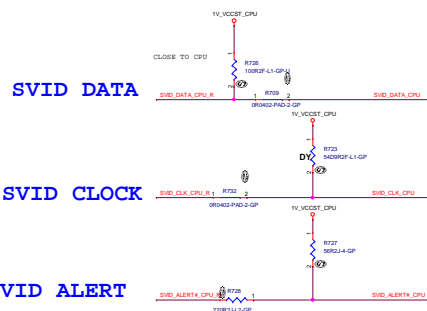
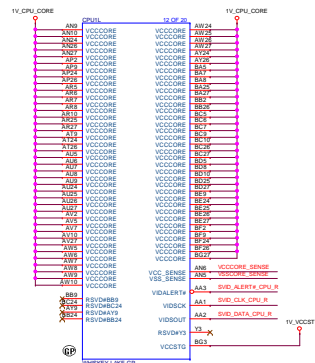


Figure 7-19. Routing Illustration for SVID Topology

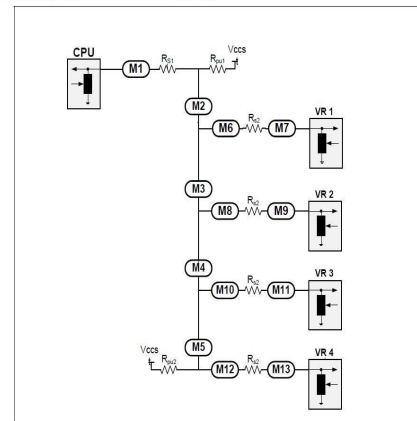


Table 7-18. SVID# Routing Guidelines (Sheet 2 of 2)

Segment	Tlne Type	Reference	Via Count	Max Length, mm		Max Length, Mills	
				Segment	Total	Segment	Total
M2	MS/SL/D5L	V55		381		15000	
M3	MS/SL/D5L	V55		102		4015.75	
M4	MS/SL/D5L	V55		102	432	4015.75	17007.9
M5	MS/SL/D5L	V55		102		4015.75	
M6	MS/SL/D5L	V55		3	3	118.11	118.11
M7	MS/SL/D5L	V55		3	3	118.11	118.11
M8	MS/SL/D5L	V55		3	3	118.11	118.11
M9	MS/SL/D5L	V55		3	3	118.11	118.11
M10	MS/SL/D5L	V55		3	3	118.11	118.11
M11	MS/SL/D5L	V55		3	3	118.11	118.11
M12	MS/SL/D5L	V55		3	3	118.11	118.11
M13	MS/SL/D5L	V55		3	3	118.11	118.11
Topology Guidelines							
SVID Signals			VIDSOUT, VIDSCK, VIDASALERT#				
VIDSOUT platform resistors			Rpu1=1000, Rpu2=1000, Ra1=0G, Ra2=10G				
VIDSCK platform resistors			Rpu1=Empty, Rpu2=450, Ra1=0G, Ra2=49.9Q				
VIDASALERT# platform resistors			Rpu1=560, Rpu2=Empty, Ra1=220D, Ra2=0G				
Platform resistors tolerances			± 5%				
Route ordering			When routing at minimum spacing route Alert between Data and Clock				
Length Matching Rules							
Length Matching between VIDSOUT and VIDSCK			± 100mils				

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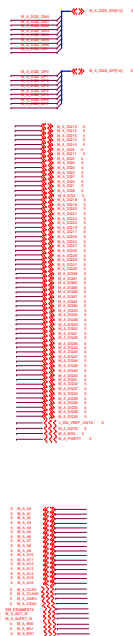
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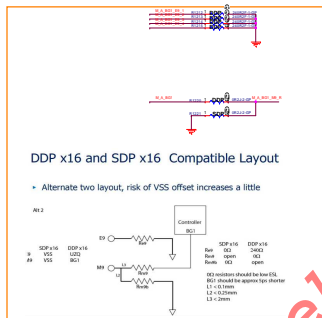
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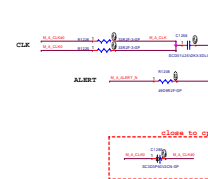
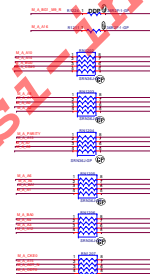


SDP & DDP SETTING

R1219-R1216 (R013)(20170911)(DWL: R1216-R1219)
SDP: 240 ohm (4x,24005,020)
SDP: 0 ohm (x3,R0034,1DL)



CBL/CEE/CIO

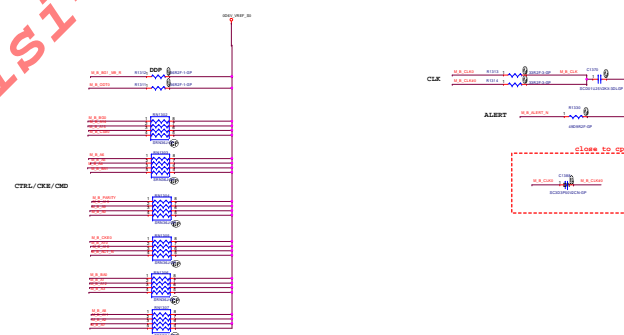
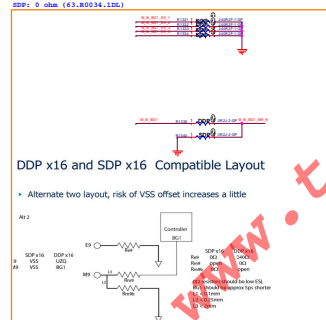
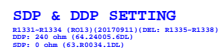
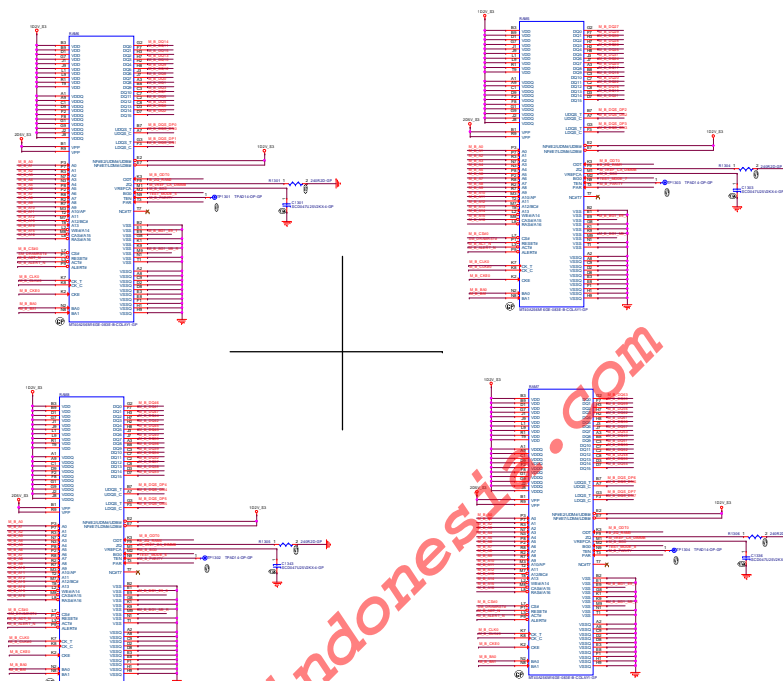
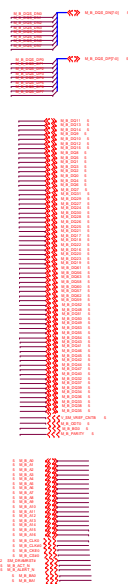


4.7.2 WHL-U DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (down)	4 per dram, as close as possible Distribute evenly across domain, close by Drams	32x 1uF (0402) (All alluPd)
	VDDQ/VDD (down)	2 per dram, as close as possible Distribute evenly across domain, close by Drams	10x 10uF (0603) (All alluPd)
	VPP	distributed along termination resistors	16x 1uF (0402)
	VTT	distributed along termination resistors	5x 10uF (0603)

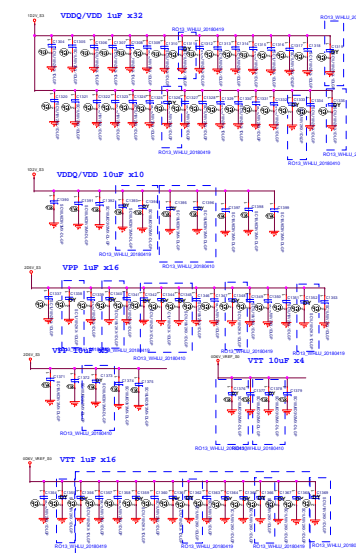


4.7.2 WHL-U DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation

Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)


Memory Configuration	Power Domain	Decoupling Location	Qty or μF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible distribute evenly across domain, close by Drams	32x 1 μF (0402) (All stuffed)
			15x 10 μF (0503) (All stuffed)
	VPP	2 per dram, as close as possible distribute evenly across domain, close by Drams	16x 1 μF (0402)
			5x 10 μF (0603)
	VTT	distributed along termination resistors distribute evenly across domain	16x 1 μF (0402) 4x 10 μF (0603)



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19,27	BPOK	CC	CC
20	NABR,307	CC	CC
18	CPU_308B_ALERTN_P1	CC	CC
18,20,81	SP1_B, CPU	CC	CC
18,20	SP1_BSP, CPU	CC	CC
18,20	SP1_N20B, CPU	CC	CC
18	H2B, BOUTD, CPU	CC	CC
20,81	ENV_R0, DT	CC	CC
8	CPDS	CC	CC
8	CPDS4	CC	CC
18	CPU_308B_ALERTN	CC	CC
20	OPP_R32, (OPP_R)000	CC	CC
18	CPU_308B_ALERTN_P1	CC	CC
21	OPP_N01	CC	CC
17	INPUT00B1	CC	CC
21	OPP_N03	CC	CC
21	OPP_0	CC	CC
20,26	KTC, D204	CC	CC
6	OPP_N07, STRAP	CC	CC

GPIO_B14 / SPKR Speaker Override	Rising edge of PCH_PWRACK	<p>The signal has a weak internal pull-down.</p> <ul style="list-style-type: none"> 0 Disable "Top Swap" mode. (Default) 1 Enable "Top Swap" mode. This inverts an address on access to SPI and firmware hub. The signal believes it reflects the alternate boot chip. However, the original boot-block "PCB" will not be able to boot. The code points from the upper 16 bits of the address to the lower 16 bits of the address (bits A15..A17 are SPI flash Programming Guide). <p>Notes:</p> <ul style="list-style-type: none"> The internal pull-down is disabled after PCH_PWRACK is high. Software will not be able to clear the "Top Swap bit" until the system is rebooted. The signal is the primary enable using the "Top Swap bit" (Bund. Device31, Function0, offset DCH[0]). This signal is in the string "v1".
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<p>GPP_B18 / GSPIO_M0SI</p>	<p>No Reboot</p>	<p>Rising edge of PCH_PWR0K</p>	<p>The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after PCH_PWR0K is high. 2. This signal is in the primary well.
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GPP_C2 / SMBALERT#	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default).</p> <p>1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support internal ATMT with TLS.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
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			<p>This signal has a weak internal pull-down. The field determines the destination of accesses to the B12S memory range. Also controllable using Host BIOS destination bit (Bios0_Dwvrt3_3). Function0, offset 0x28, bit 6.</p> <table><thead><tr><th>Bit 6</th><th>Do not BIOS Destination</th></tr></thead><tbody><tr><td>0</td><td>SPI (Default)</td></tr><tr><td>1</td><td>LPC</td></tr></tbody></table>	Bit 6	Do not BIOS Destination	0	SPI (Default)	1	LPC
Bit 6	Do not BIOS Destination								
0	SPI (Default)								
1	LPC								
GPP, B12, PCH2_HDQS	Do not B12 Do not B12 Do not B12	Rising edge of PCH2_HDQS B12	Notes: <ol style="list-style-type: none">The internal pull-down is disabled after BIOS. B12 is high.When the internal pull-down is disabled, SPI may still be passed on LNC, but all platforms are required to have a pull-up connected directly to the BIOS SPI pin to avoid excessive transition in input to LNC.The B12 signal is sent to LNC by functional group or by functional group.Do not affect SPI accesses initiated by Intel I/O or Freescale QSPI LAN.						



			<p>This signal has a weak internal pull-down.</p> <p>0 = LPC is selected (for EC). (Default)</p> <p>1 = eSPI is selected (for EC).</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. <p>Warning: If this strap is configured to '0' (eSPI is disabled), the eSPI Flash Sharing Mode strap must be configured to '0' as well (SAFS is disabled)</p>
GPP_CS / SMIOALERT#	eSPI or LPC	Rising edge of RSMRST#	



SPIO_MOST	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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GPP_D12 / ISH_SPI_MOSI / GSP12_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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GPP_823 / SMILATER# / PCCHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	<p>This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCCHOT# and strap low, a 150k pull-up is needed to ensure it does not override the internal pull-down strap sampling. <p>This signal is in the primary well.</p>
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SPI0_I02	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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SPIO_I03	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
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HDA_SDP0 / I2SD0_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Enable security measures defined in the Flash Descriptor (default)</p> <p>1 = Disable Flash Descriptor Security (<u>write</u>). The pins should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p>Notes:</p> <p>The internal pull-down is disabled after PCH_PWROK is high. This signal is in the primary wall.</p>
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GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. Notes: 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
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GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
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<p>GPP_E23 / DDPD_CTRLDATA</p>	<p>Display Port D Detected</p>	<p>Rising edge of PCH_PWROK</p>	<p>This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.</p>
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GPP_H17	Reserved	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
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GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.</p> <p>0 = 38.4 XTAL frequency selected. (Default)</p> <p>1 = 24MHz XTAL frequency selected.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
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GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
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INPUT3VSEL	3.0V Select	<p>Input pin must always be driven to a valid logic level</p> <p>External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5%</p> <p>Note: This strap should only be used for specific targeted iS battery systems.</p>
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GPD7	Reserved	Rising edge of DSW_PWROK This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling	External pull-up is required. Recommend 100K.
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<p>GPP_H23</p>	<p>eSPI Flash Sharing Mode</p>	<p>Rising edge of RSMRST#</p> <p>This signal has a weak internal pull-down.</p> <p>0 = Master Attached Flash Sharing (MAFS) enabled (Default)</p> <p>1 = Slave Attached Flash Sharing (SAFS) enabled.</p> <p>Notes:</p> <ul style="list-style-type: none"> The internal pull-down is disabled after RSMRST# de-asserts. This signal is in the primary well. <p>Warning: This strap must be configured to '0' (SAFS is disabled) if the eSPI or JLC strap is configured to '0' (eSPI is disabled).</p>
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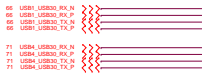
[Now Only] PHYSICAL_DEMO_ENABLED (DPE PRIVACY)	
CMD[0]	0 : DISABLED SET DPE_ENABLED BIT IN DEMO INTERFACE ROM 1 : DISABLED



<pre> DISPLAY POST PRESENCE STRAP </pre>	
CRQ[4]	<pre> 0 = SUCCESS An external Display Post device is connected to the Embedded Display Port. 1 = STRAPED (Default) No Physical Display Post attached to Embedded DisplayPort?. No connect for disble. </pre>



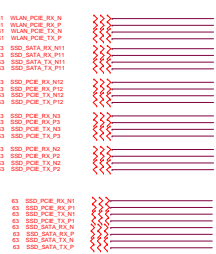
USB3.0



USB2.0



PCIe



WLAN

2ND M.2

SSD



USB 2.0 Table

Pair	Device
1	USB3.0 ports (1000)
2	N/A
3	N/A
4	Type-C
5	Fingerprint
6	CAMERA
7	Card Reader
8	N/A
9	N/A
10	WLAN (BT)

Premium / Base	USB2 #1	USB2 #2	USB2 #3	USB2 #4	USB2 #5	USB2 #6	USB2 #7	USB2 #8 (only)	USB2 #9 (only)	USB2 #10
CY18 Port Mapping	External Port / Type-C #1	External Port / Type-C #2	External Port / Type-C #3	External Port / Type-C #4	Fingerprint	Camera	Card Reader			BT
RO13_WHL	USB2.0 (IO board)			TYPE-C	Fingerprint	Camera				BT

Premium / Base	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0	USB3.0
PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
CY18 Port Mapping	External Port / Type-C #1	External Port / Type-C #2	External Port / Type-C #3	External Port / Type-C #4	External Port / Type-C #5	External Port / Type-C #6	External Port / Type-C #7	External Port / Type-C #8	External Port / Type-C #9	External Port / Type-C #10	External Port / Type-C #11	External Port / Type-C #12	External Port / Type-C #13	External Port / Type-C #14	External Port / Type-C #15	External Port / Type-C #16
RO13_WHL	USB3.0 (IO board)	NA	NA	TYPE-C	NA	NA	WLAN	Optane (PCIe/SATA)	Optane (PCIe)	SSD (PCIe)	SSD (PCIe)	SSD (PCIe)	SSD (PCIe)	SSD (PCIe)	SSD (PCIe)	SSD (PCIe)

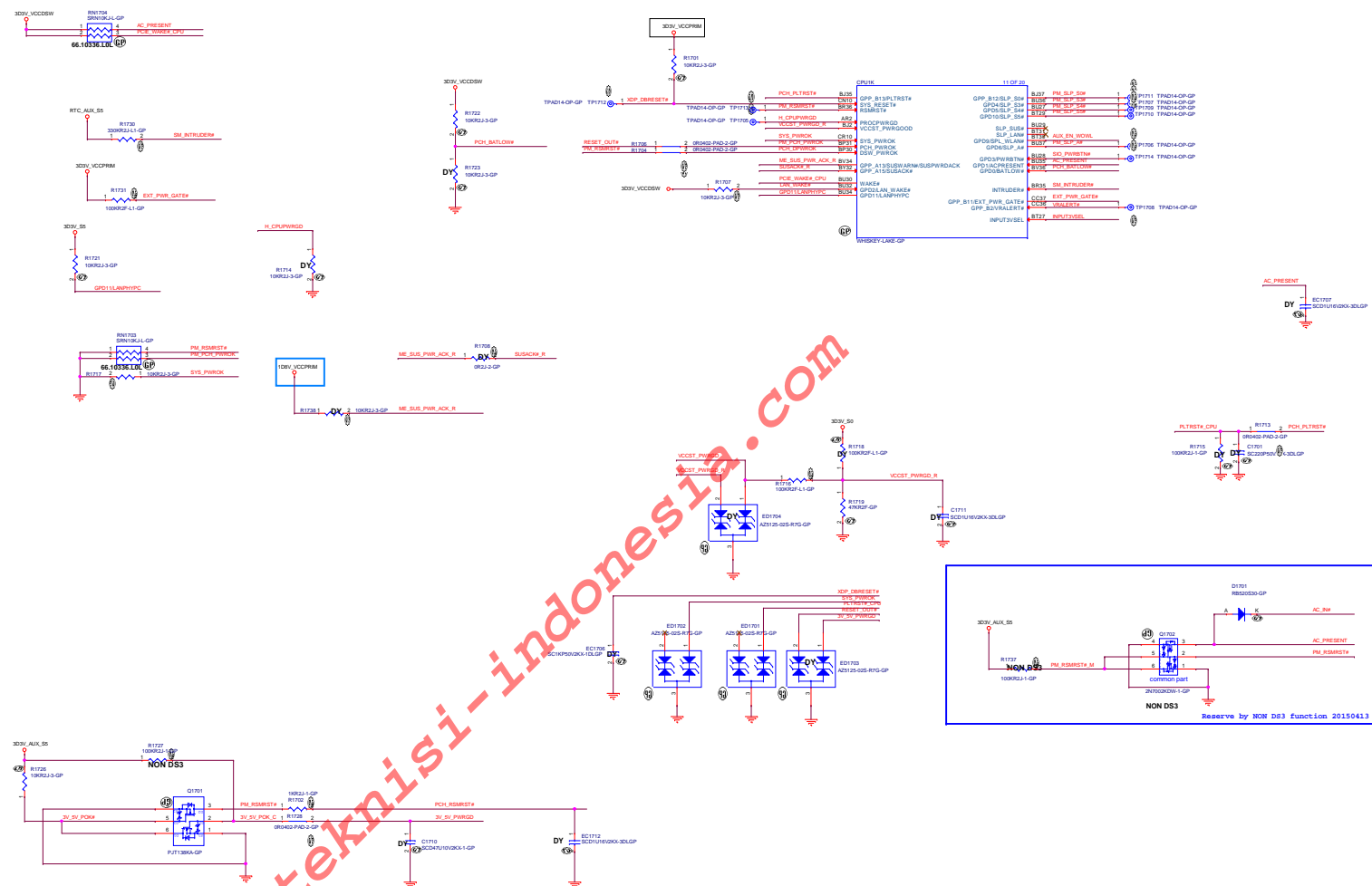
6.3 PCH PCI Express* Interface Design Guidelines

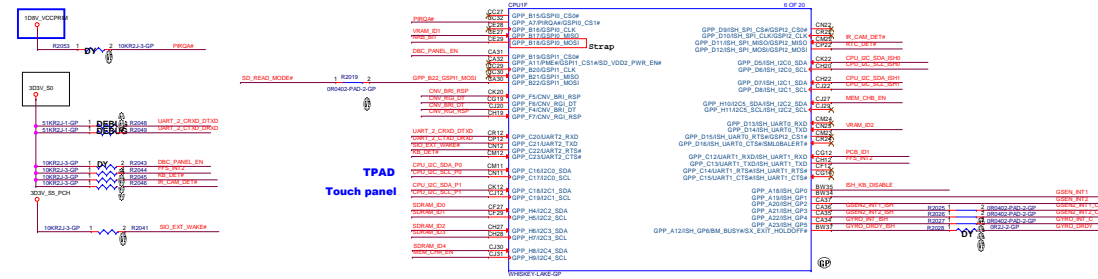
6.3.1 PCH PCI Express* Interface Configuration Details

Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3	PCIe* Controller #4
Flex I/O Lane	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
PCIe* Lane	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
PCIe* Lane	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
PCIe* Lane	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

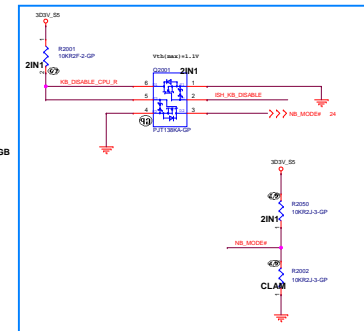
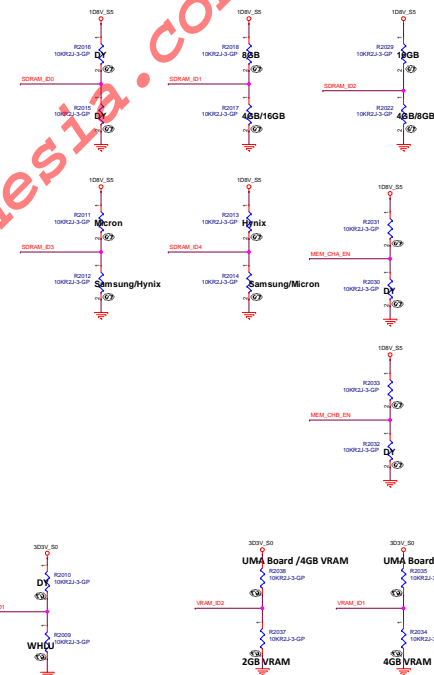
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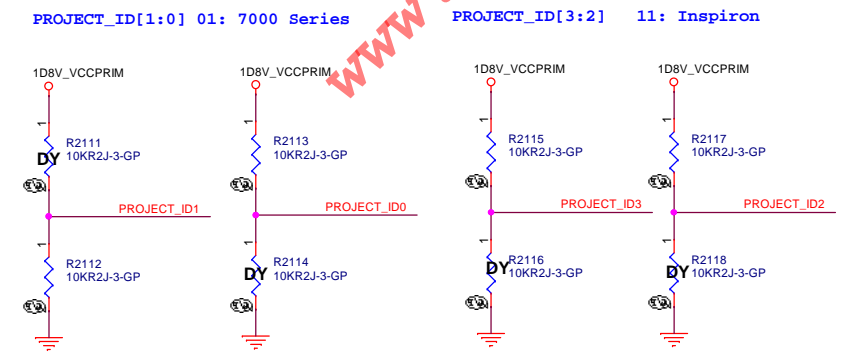
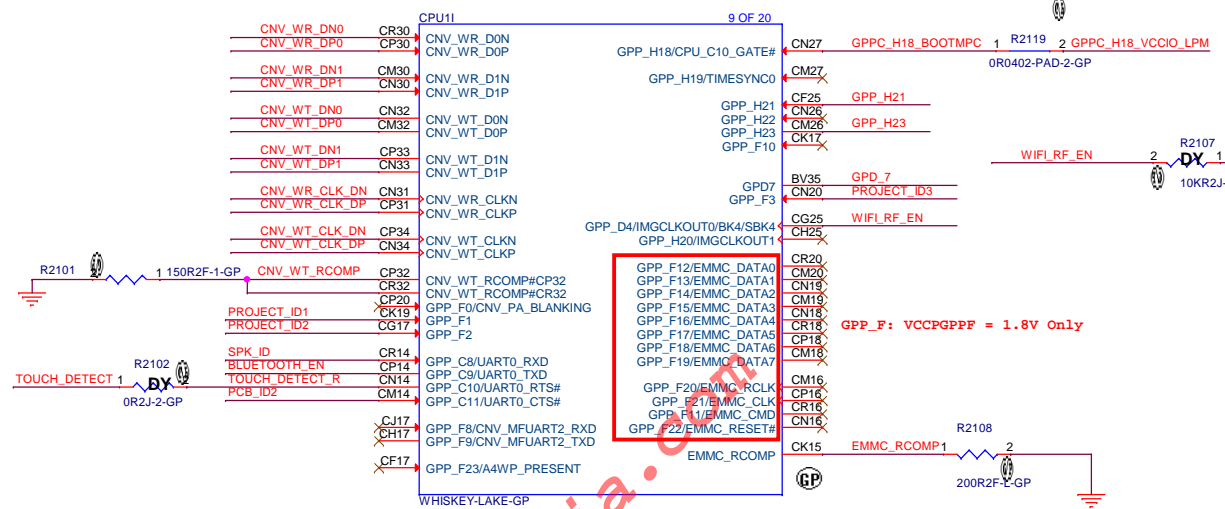
RAM ID						
Vender	MEM_CONFIG [0]	MEM_CONFIG[1:2]	MEM_CONFIG[3:4]	Mem. PN	Wistron. P/N	Capacity
Samsung	NA	01	00	K4AAG16SWB-MCRC	TBD	16G
Micron	NA	01	10	MT40A1G16KNR-075E	TBD	16G
Hynix	NA	01	01	H5ANAG6NAMR-UHC	TBD	16G
Samsung	NA	10	00	K4A8G16SWB-BCRC	TBD	8G
Micron	NA	10	10	MT40A512M16LY-075E	TBD	8G
Hynix	NA	10	01	H5AN8G6NAPR-UHC	TBD	8G
Samsung	NA	00	00	K4A4G16SWE-BCRC	072.44165.0B0U	4G
Micron	NA	00	10	MT40A256M16GE-083E	072.40256.0A0U	4G
Hynix	NA	00	01	H5AN4G6NAMR-UHC	TBD	4G

MEM_CONFIG[4:3]	On-board memory config for chip vendor	11	DIMM Design
		10	Hynix
		01	Micron
		00	Samsung
MEM_CONFIG[2:1]	On-board memory config for total memory size per channel	11	4GB
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	Reserved (non-use)		



Main Func = PCH

- 61 WIFI_RF_EN <<<
- 29 SPK_ID >>>
- 61 BLUETOOTH_EN <<<
- 55 TOUCH_DETECT <<<
- 20 PCB_ID2 <<<
- 15 GPP_H21 <<<
- 15 GPP_H23 <<<
- 15 GPD_7 <<<
- 61 CNV_WT_CLK_DP >>>
- 61 CNV_WT_CLK_DN >>>
- 61 CNV_WT_DP0 >>>
- 61 CNV_WT_DN0 >>>
- 61 CNV_WT_DP1 >>>
- 61 CNV_WT_DN1 >>>
- 61 CNV_WR_CLK_DP >>>
- 61 CNV_WR_CLK_DN >>>
- 61 CNV_WR_DP0 >>>
- 61 CNV_WR_DN0 >>>
- 61 CNV_WR_DP1 >>>
- 61 CNV_WR_DN1 >>>
- 40 GPPC_H18_VCCIO_LPM <<<
- 18 PROJECT_ID0 <<<

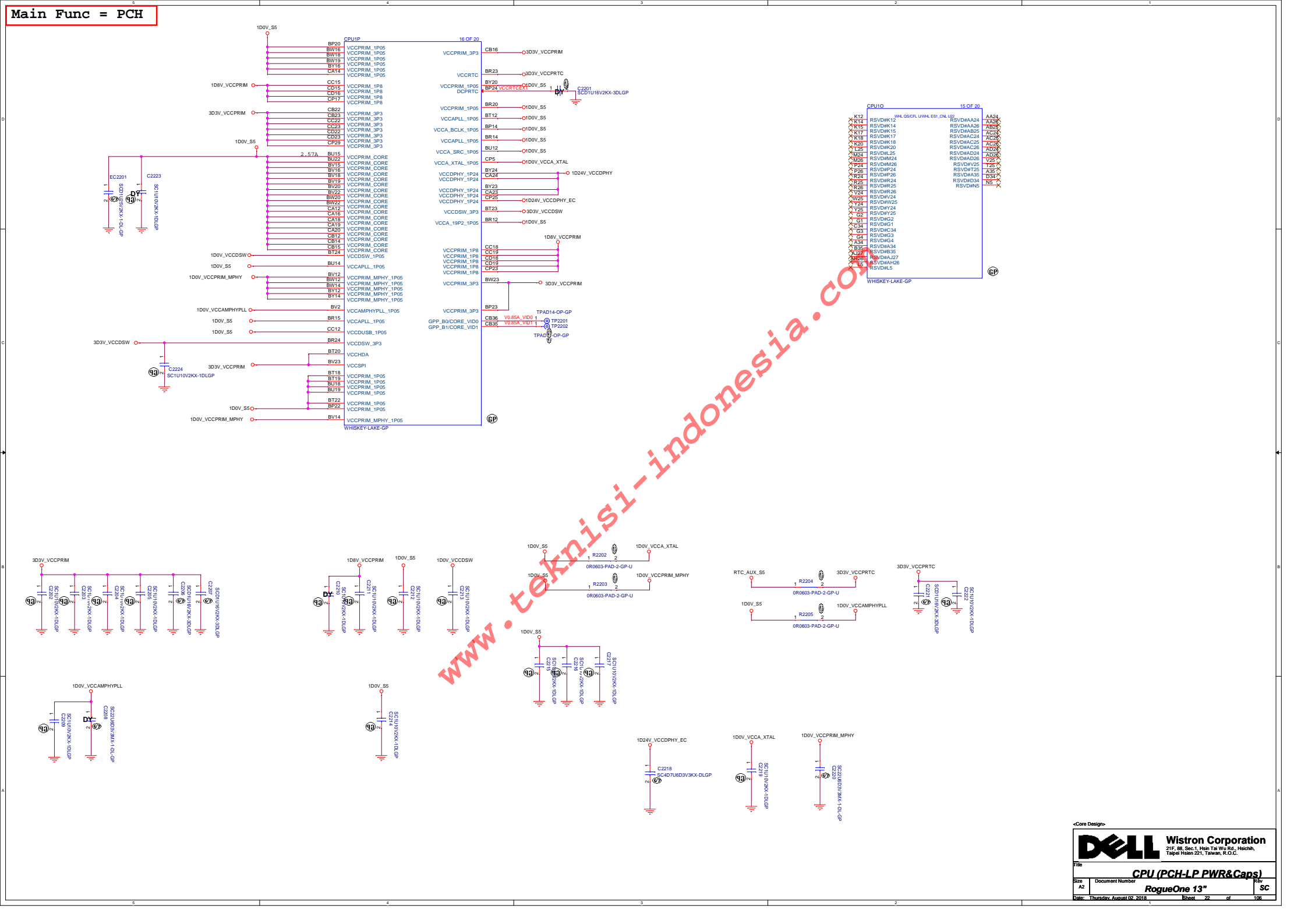


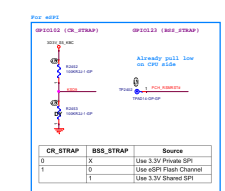
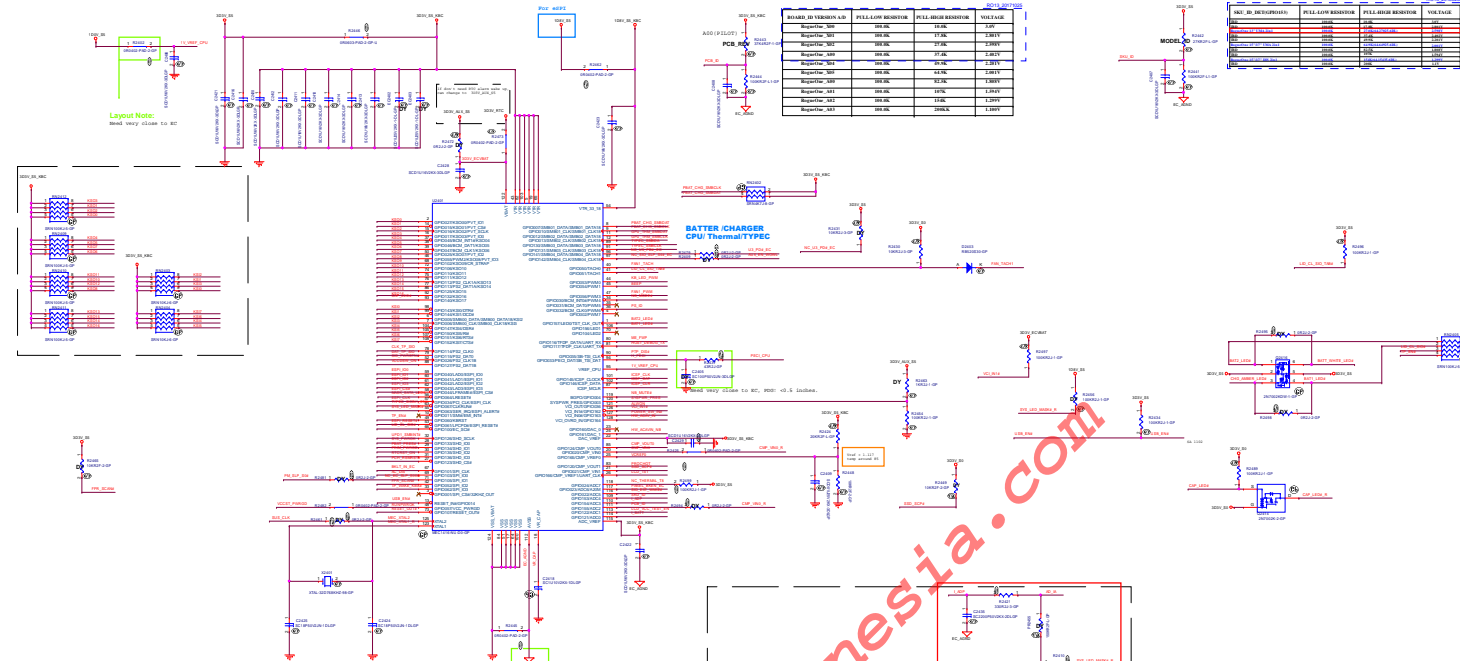
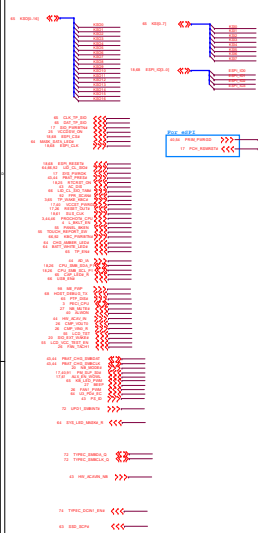
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Title: **CPU (EMMC/CNVi)**

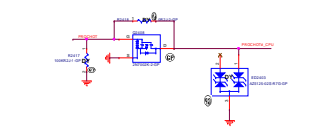
Size: A3	Document Number: RogueOne 13"	Rev: SC
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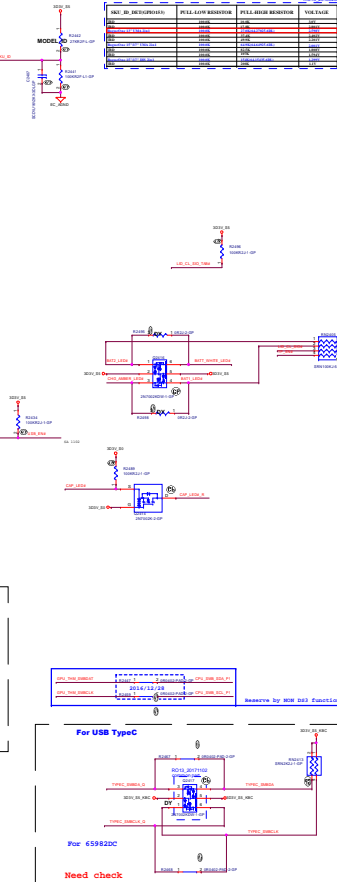


CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use 65V Flash Channel
1	1	Use 3.3V Shared SPI

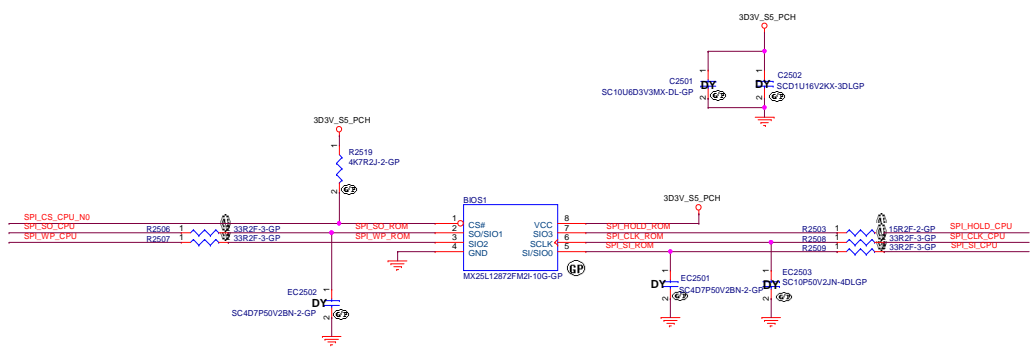
Note: If the vSPI Flash Channel is used for booting, the vSPI pin must be used as boot channel. If the vSPI pin is used for booting, then any unused vSPI pin may be used for booting.



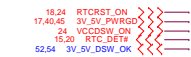
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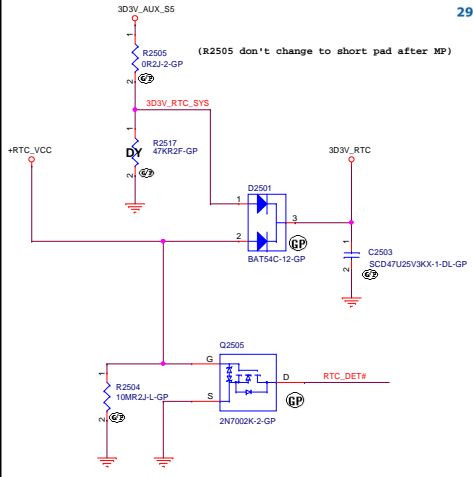
Main Func = SPI Flash



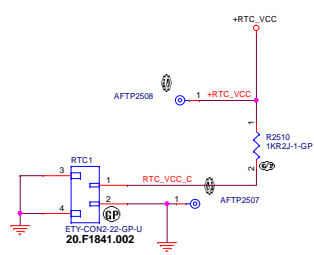
Main Func = RTC



Delivery Voltage 3.19V

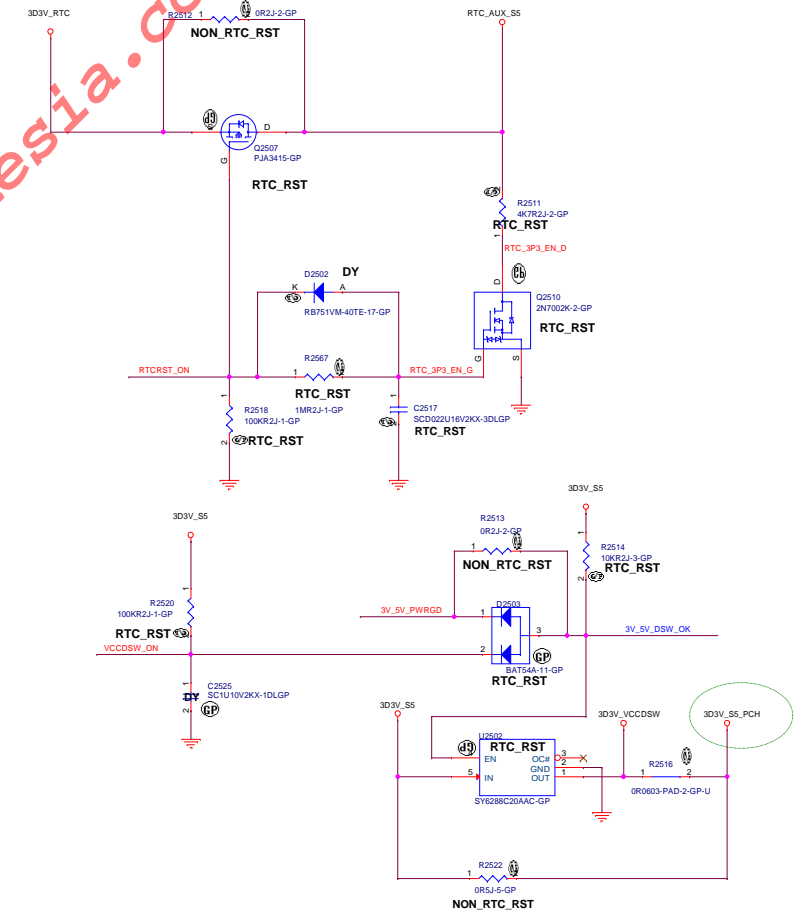


RTC



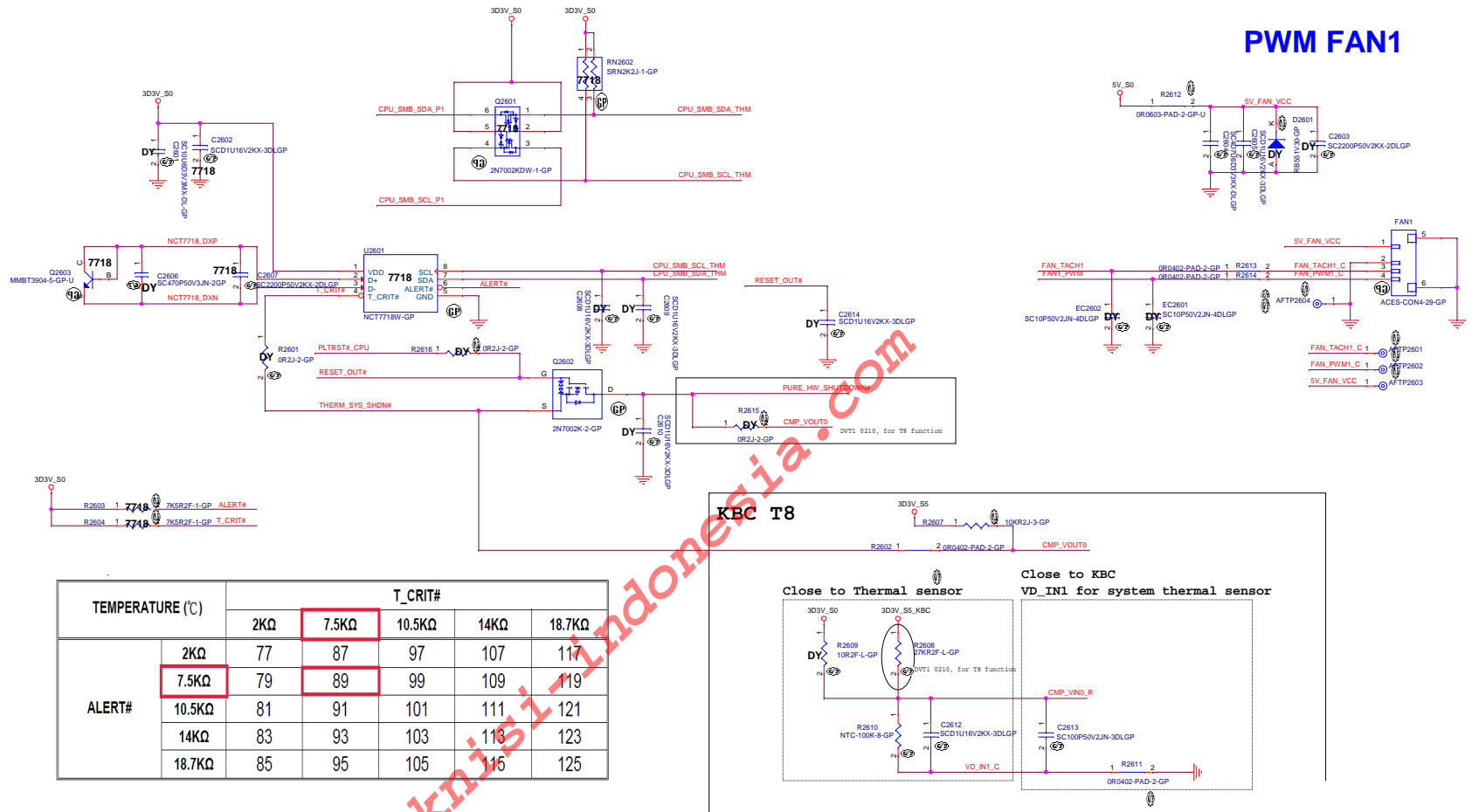
29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

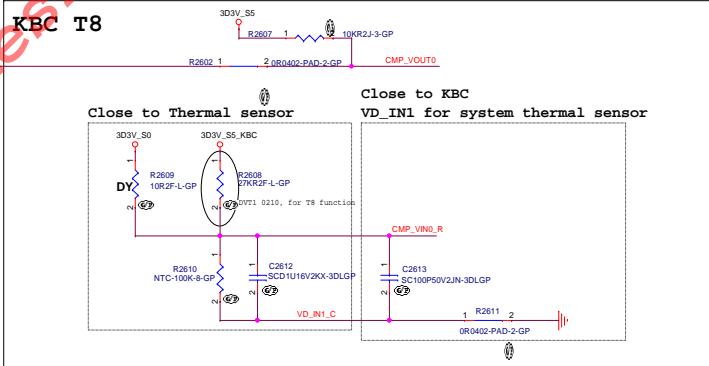


Main Func = Thermal Sensor

- 18,24 CPU_SMB_SDA_PX
- 18,24 CPU_SMB_SCL_PX
- 17,61,63,91 PLTRST#_CPU
- 17,24 RESET_OUT#
- 40 PURE_HW_SHUTDOWN
- 24 FAN1_PWM
- 24 CMP_VOUT0
- 24 CMP_VIN0_R

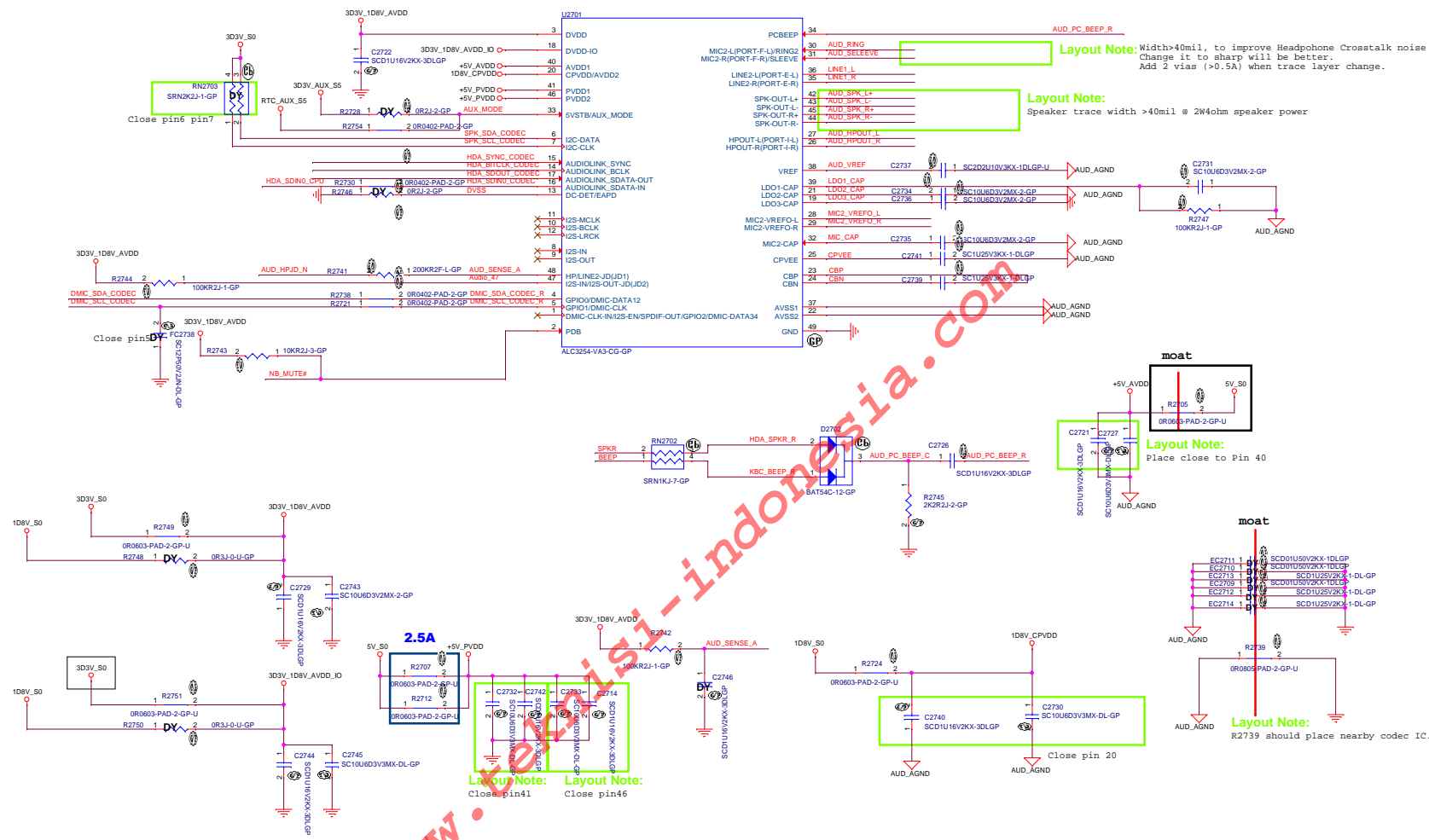


TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Main Func = Audio

- 19 HDA_SYNC_CODEC
- 19 HDA_BITCLK_CODEC
- 19 HDA_SDOOUT_CODEC
- 19 HDA_SDN0_CPU
- 55 DMIC_SDA_CODEC
- 55 DMIC_SCL_CODEC
- 1519 SPKR
- 24 BEEP
- 29 MIC2_VREF0_L
- 29 MIC2_VREF0_R
- 29 AUD_SPK_L+
- 29 AUD_SPK_L-
- 29 AUD_SPK_R+
- 29 AUD_SPK_R-
- 29 AUD_SELEEVE
- 29 LINE1_L
- 29 LINE1_R
- 29 AUD_HPUD_L
- 24 NB_MUTE#
- 29 AUD_HPOUT_L
- 29 AUD_HPOUT_R



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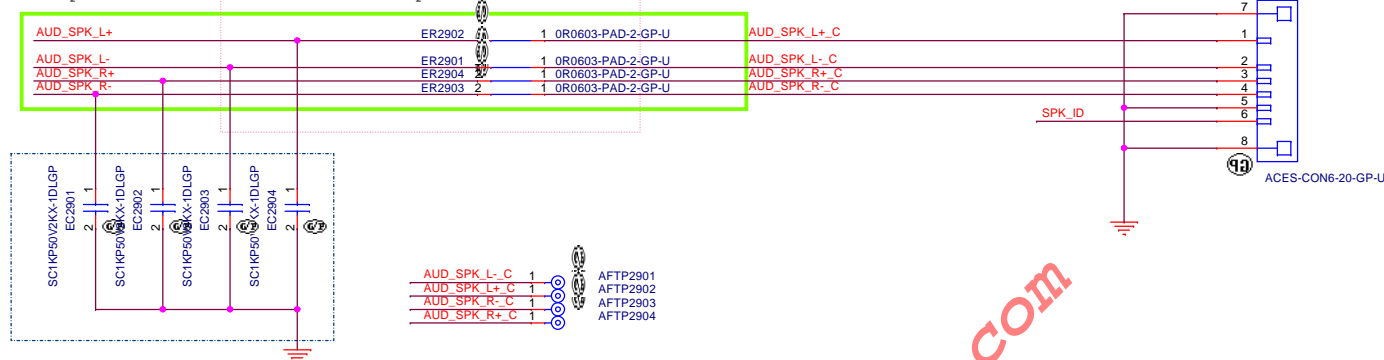
Main Func = Audio

27 AUD_SPK_L+ >>>
27 AUD_SPK_L- >>>
27 AUD_SPK_R+ >>>
27 AUD_SPK_R- >>>

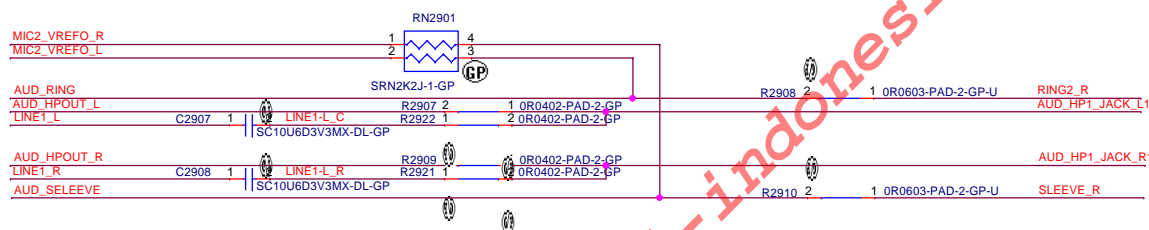
21 SPK_ID <<<
27 MIC2_VREFO_R <<<
27 MIC2_VREFO_L <<<
27 MIC2_RING <<<
27 AUD_HPOUT_L <<<
27 LINE1_L <<<
27 AUD_HPOUT_R <<<
27 LINE1_R <<<
27 AUD_SELEEVE <<<
66 RING2_R <<<
66 AUD_HP1_JACK_L1 <<<
66 AUD_HP1_JACK_R1 <<<
66 SLEEVE_R <<<
66 JACK_PLUG <<<
27 AUD_HPJD_N <<<

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

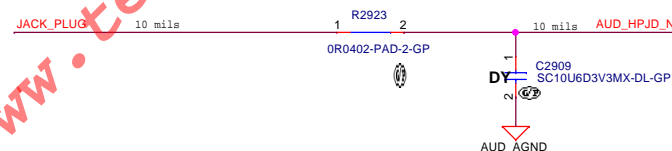


CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_DET#_CON



Delay circuit

(JACK_PLUG_DET: on IO Board)



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Audio IO

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Title LAN RTL8106			
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XFOM&RJ45			
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Card Reader-RTS5170			
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Title


USB switch

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USB30

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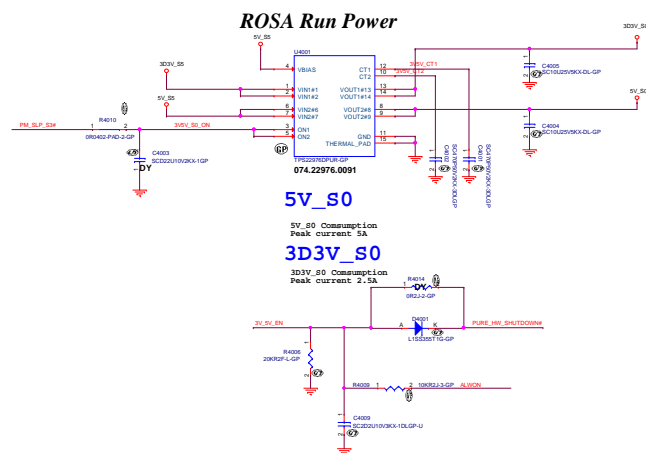
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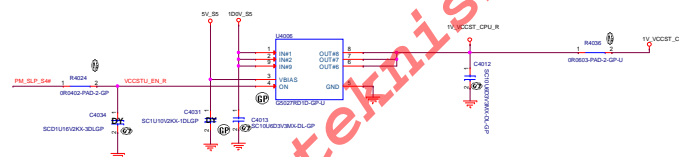
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[illegible]

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

[illegible][illegible]

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Title Connected_Standby(1/2)+DS3		
Size A4	Document Number RogueOne 13"	Rev SC
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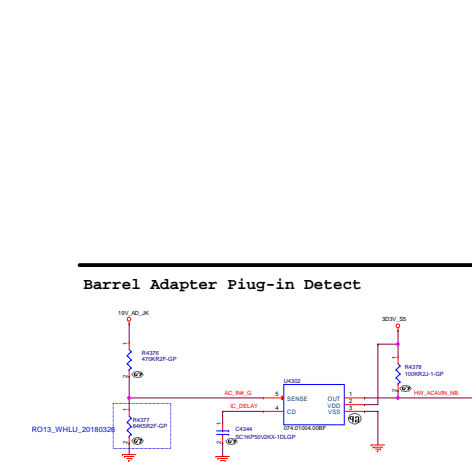
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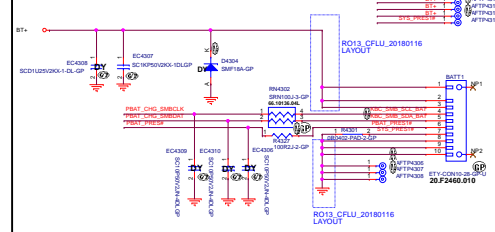
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Title Connected_Standby(2/2)			
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24 HW_ACAVN_NB <<<—
24 PS_ID <<<—
17,44 AC_BW >>>—
.44 PBAT_CHG_SMBCLK <<<<<
.44 PBAT_CHG_SMBDAT <<<<<
24,44 PBAT_PRES# <<<<<



Batt Connector



Placement: Close to Ratt Connector

2nd = 75.00099.KTD
3rd = 75.00099.KTD
4th = 75.00099.KTD

2nd = 75.00099.DTD
3rd = 75.00099.DTD
4th = 75.00099.DTD

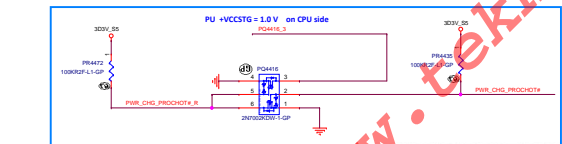
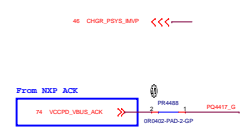
ED4306
ED4306
ED4306

DY
DY
DY

75.00099.KTD
75.00099.DTD
75.00099.KTD
75.00099.DTD
75.00099.KTD
75.00099.DTD

20V, AUX, BNC

RO13_20170822
D4304-D4306 change to ED4304-ED4306 and DY.



PROG-END (RESISTIVE Ω)				DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACTIVATION Rng(A)
MIN	TYP	MAX	CELL #			
0			1	733kHz	No	0.475
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.475
28.0				733kHz	Yes	0.475
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.475
61.9				1MHz	No	0.475
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.475
105			3	733kHz	No	0.475
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.475
162				733kHz	Yes	0.475
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.475
237				1MHz	No	0.475
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.475
348			1	733kHz	No	0.475

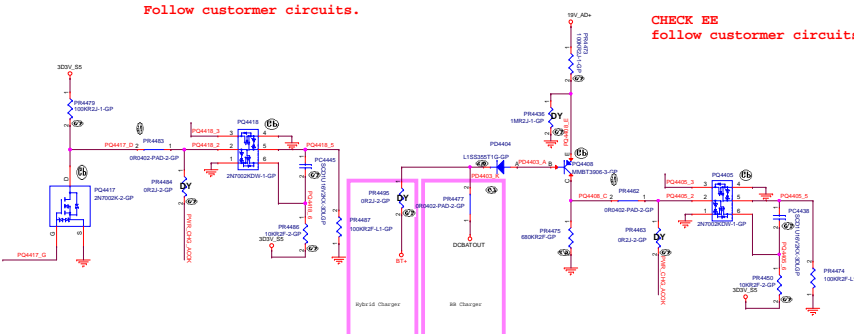
75.87333.071 CSD87330
HS-
Vgs @ 5V,
Id = 15A,
Rds(on) = 9.45mohm,
LS-
Vgs @ 5V,
Id = 15A,
Rds(on) = 3.6mohm.

84.07121.037 SI7121DN
Rds(on) = 24-30 mohm,
Vgs=10V, I-D = 12A,
Qg = 43nC
Vgs=± 25V, Vds=-30V,
I-D=16A

Need EE Check

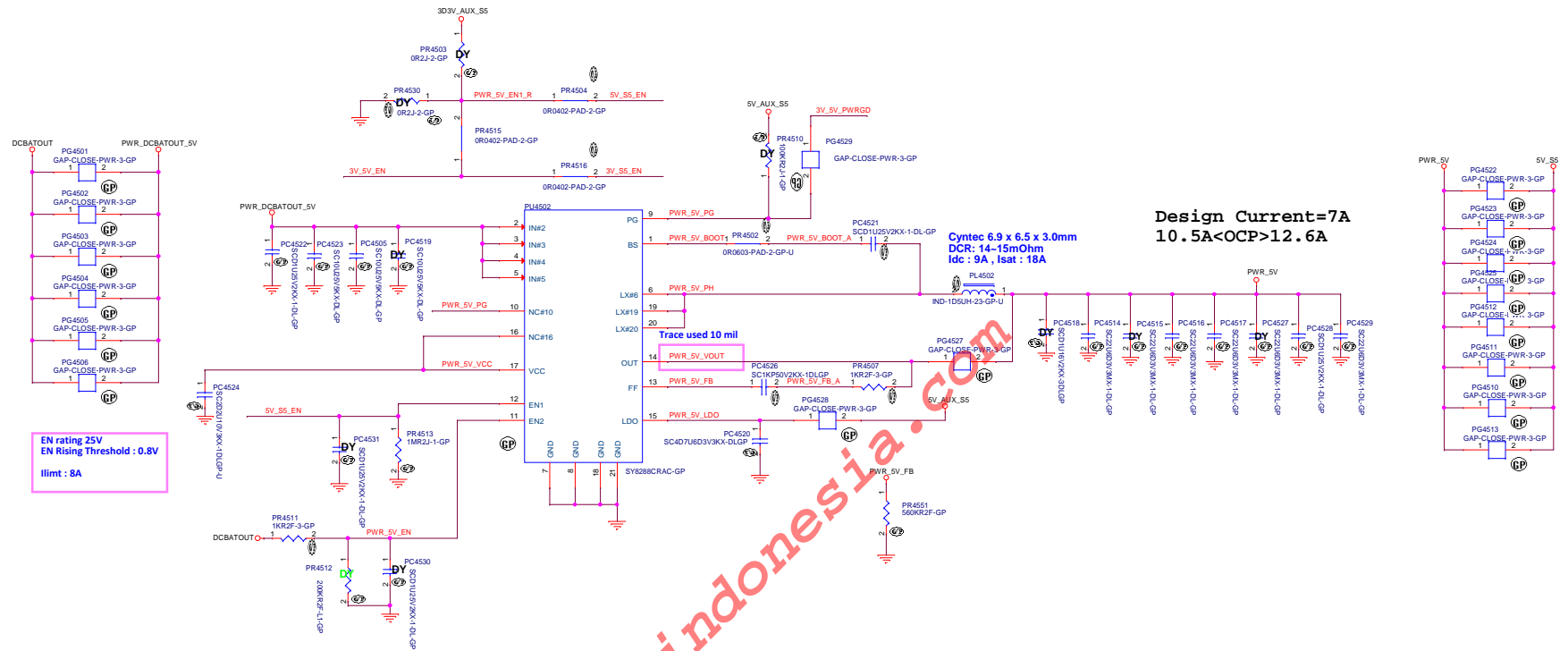
Follow customer circuits.

CHECK EE

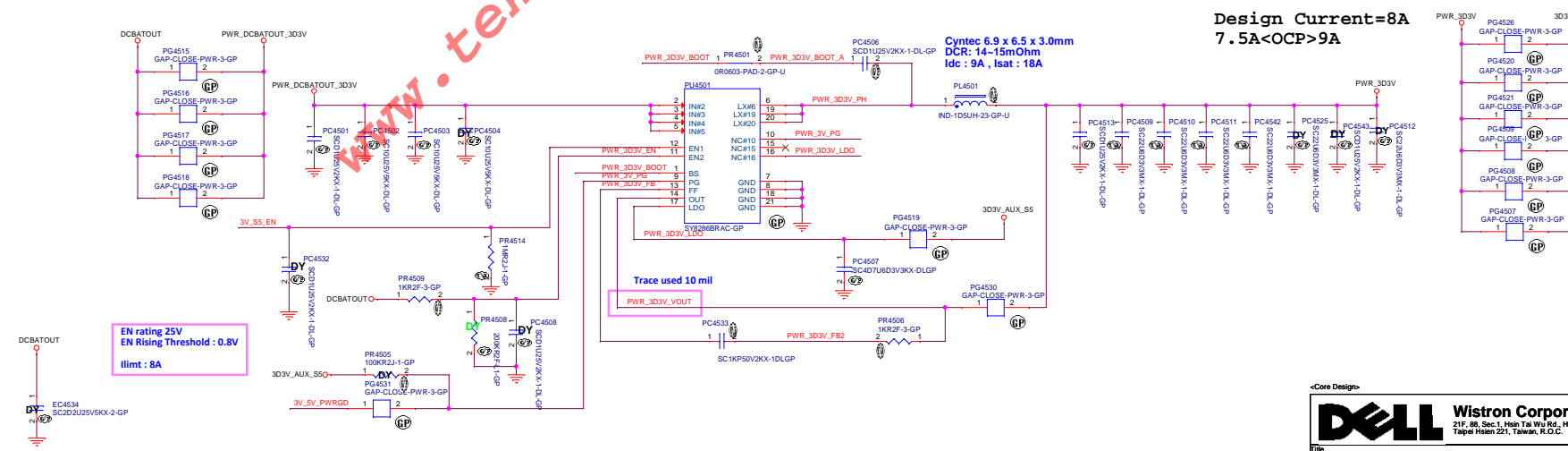


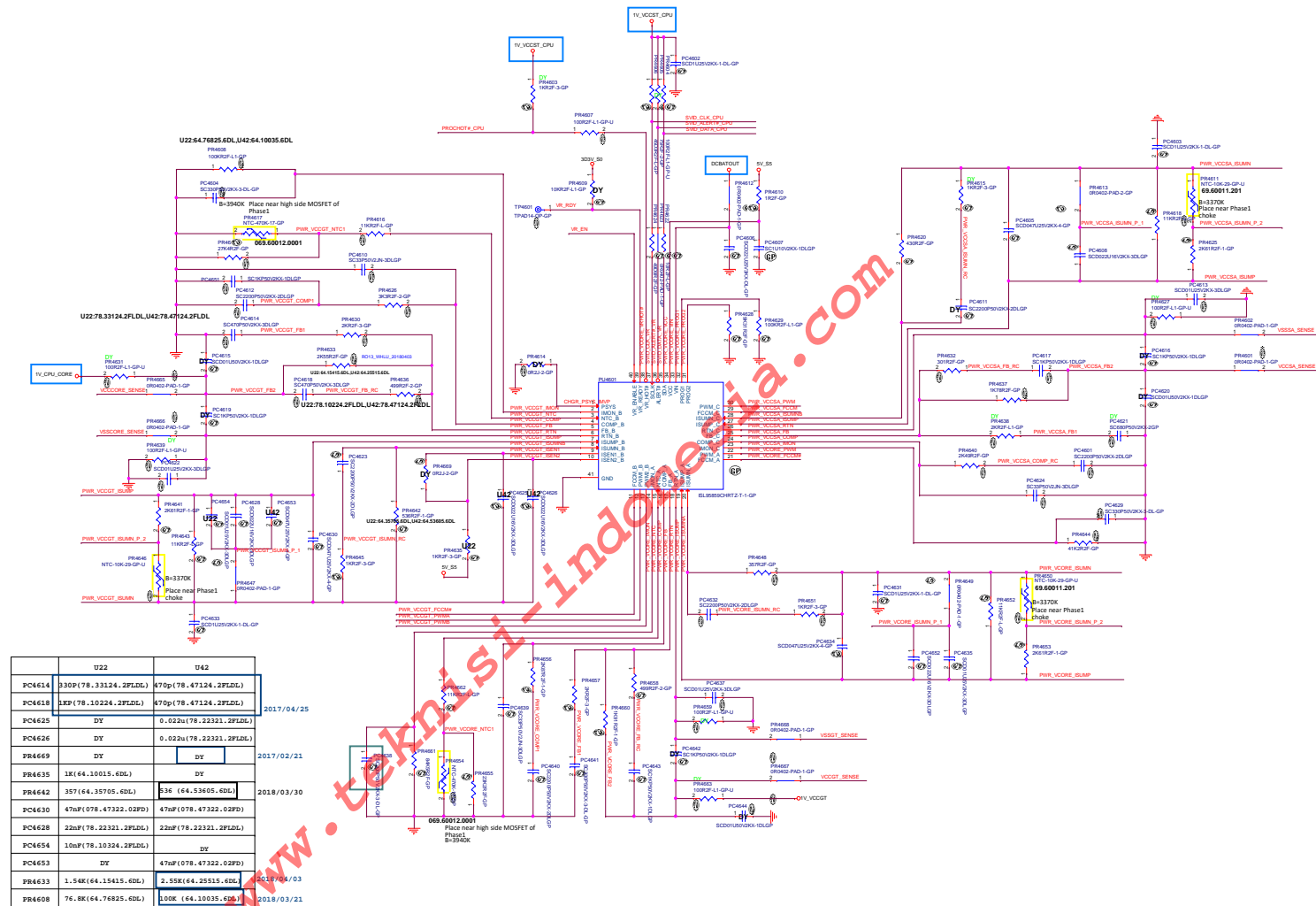
Main Func = PWR.Plane.Regulator_5V

40 3V_SS_EN >>>
17,25,40 3V_SS_PWRGD



Main Func = PWR.Plane.Regulator_3D3V





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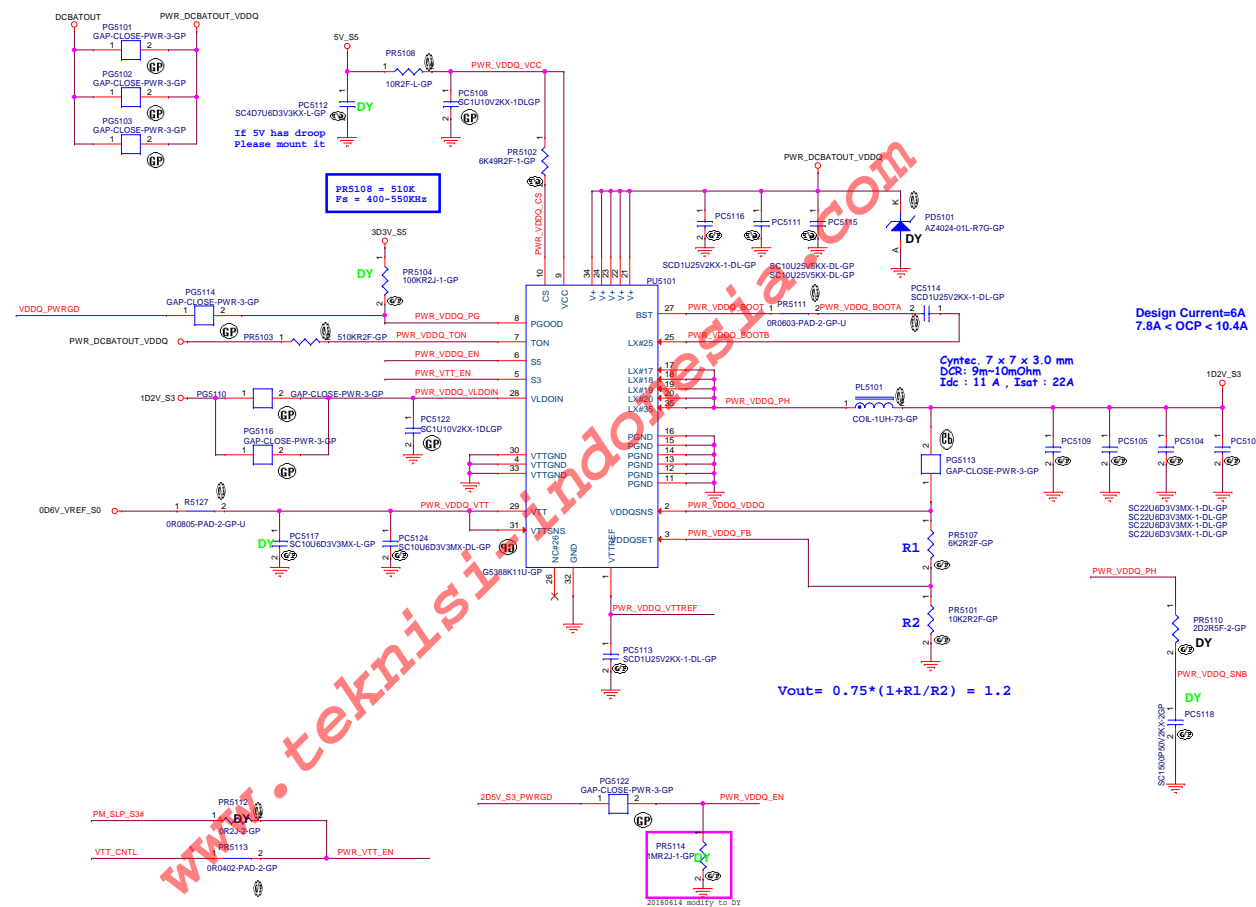


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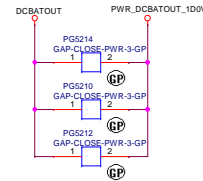
Title **NCP81210MN_CPU_VCCGTUS**

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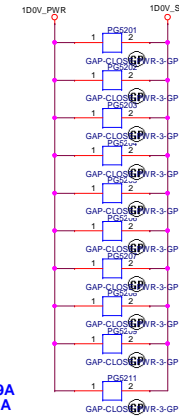
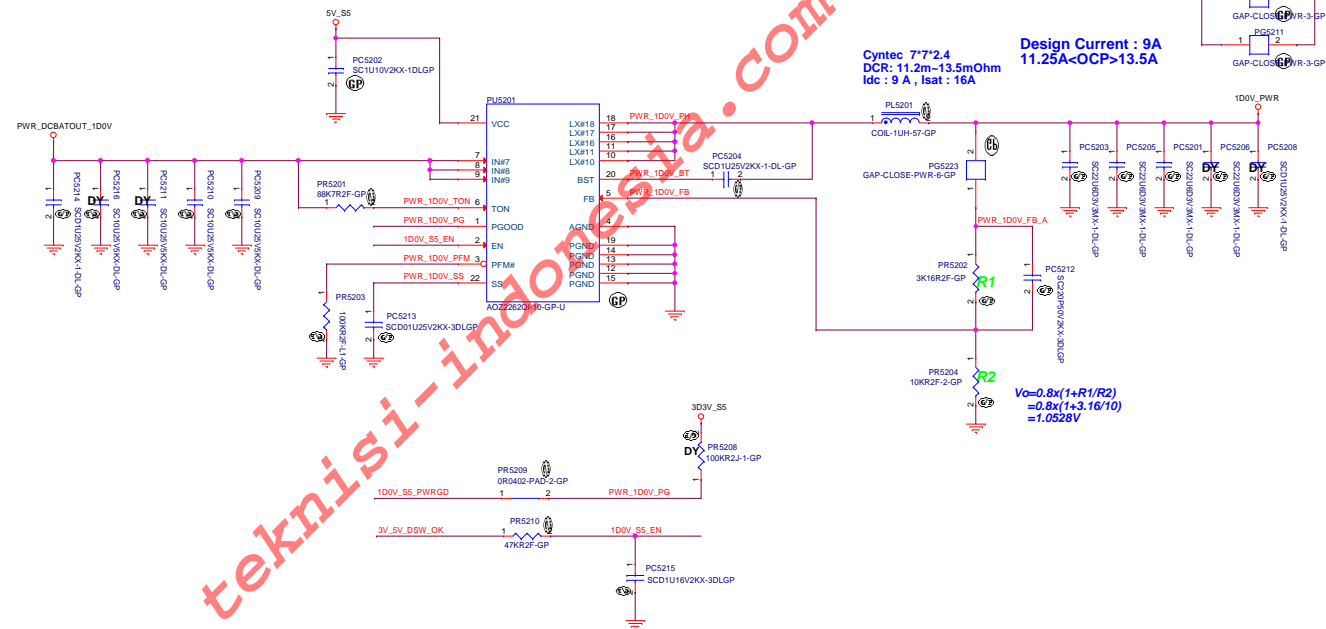
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40 100V_SS_PWRGD <<<<==
25.54 3V_5V_DSW_OK <<<<==



AOZ2262 for 1D0V



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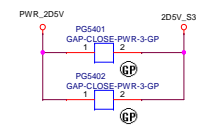
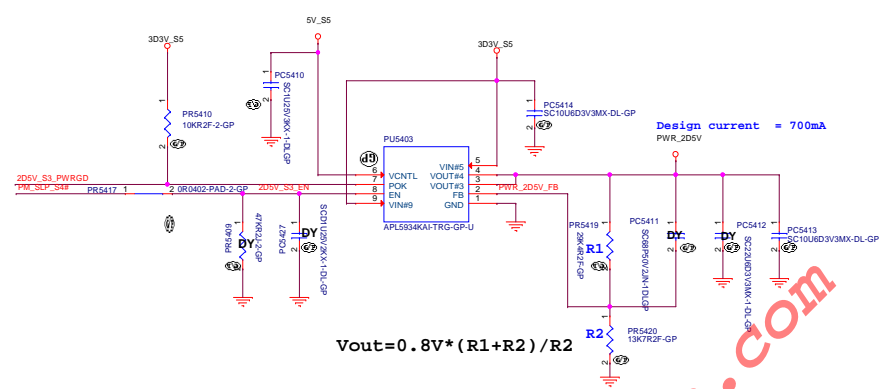
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APL5930 for 2D5V

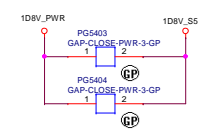
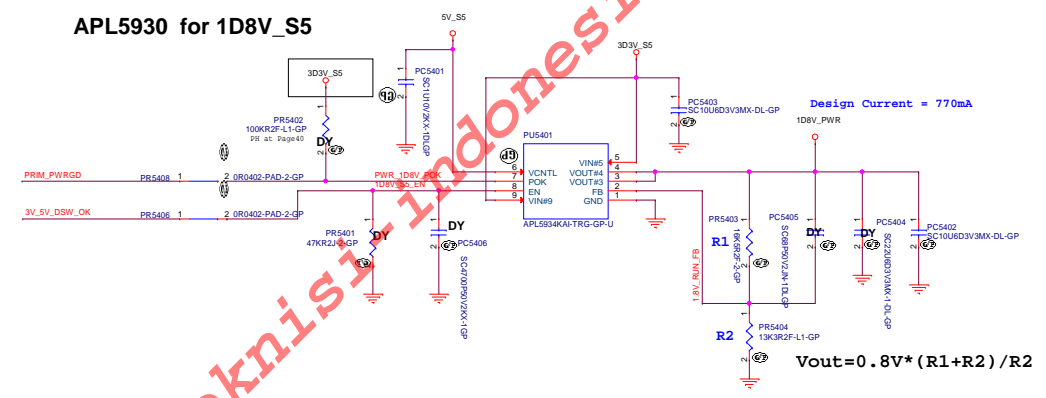
51 2D5V_S3_PWRGD
17.40.92 PM_SLP_S4#



$$V_{out} = 0.8V * (R1 + R2) / R2$$

APL5930 for 1D8V_S5

24.40 PRIM_PWRGD
25.52 3V_SV_DSW_OK



$$V_{out} = 0.8V * (R1 + R2) / R2$$


[illegible]

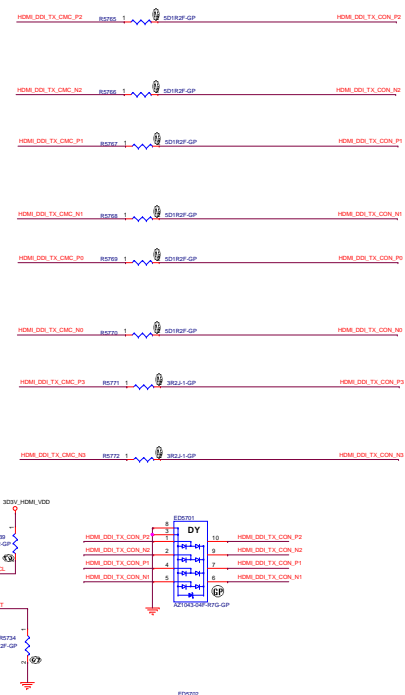
Starload height limite change to 0603 package
2015/09/30 modify

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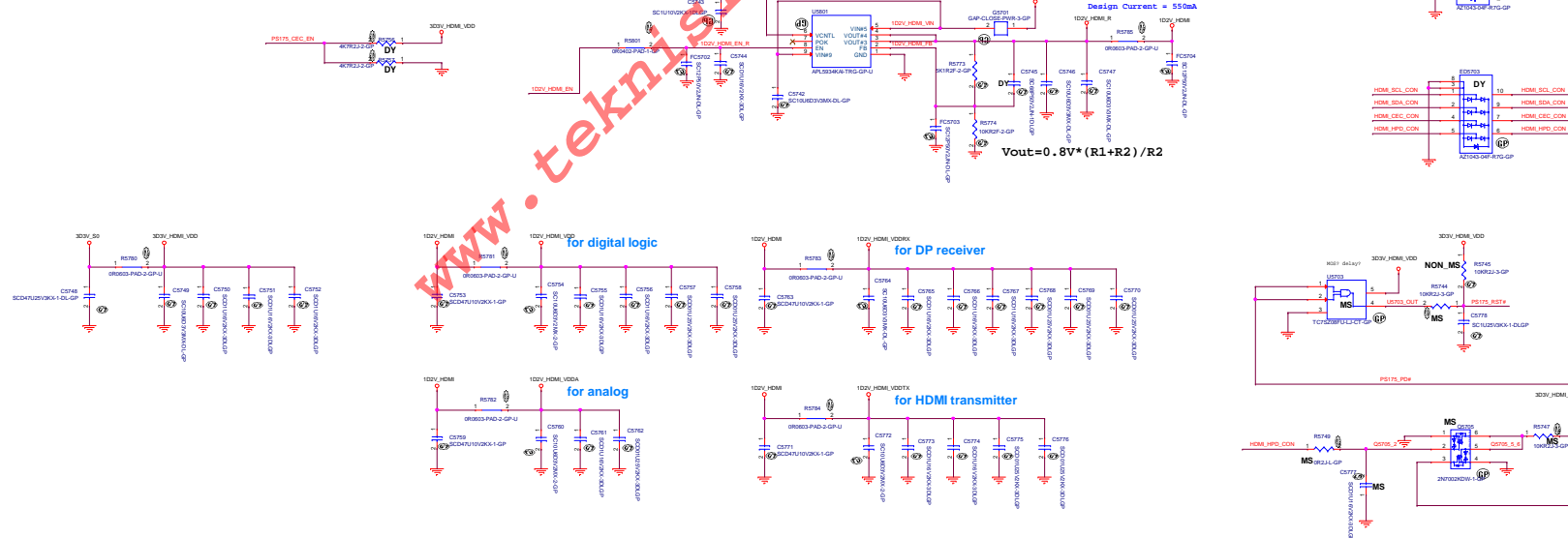
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Title CRT			
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50mA

$$V_{out} = 0.8V \cdot (R1 + R2) / R2$$



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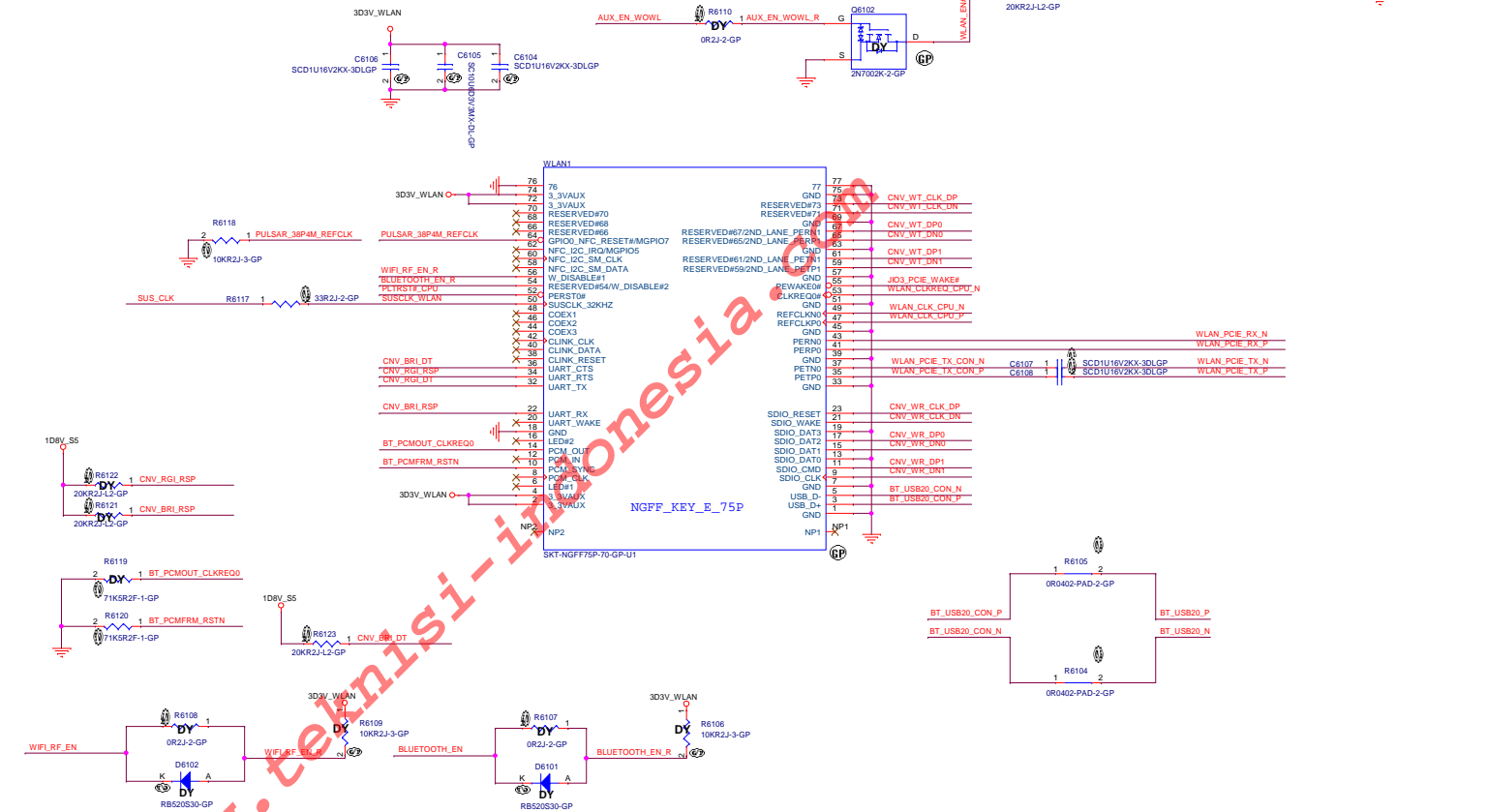
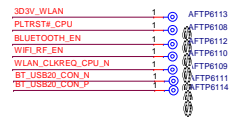
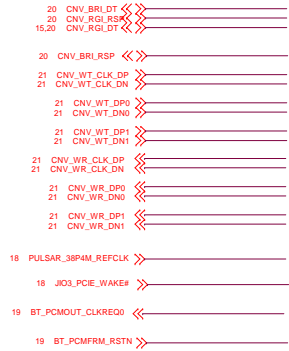
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Title (Reserved)			
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```

16  BT_USB20_N  >>>
16  BT_USB20_P  >>>
21  BLUETOOTH_EN >>>
21  WIFI_RF_EN  >>>
17,26,63,91  PLTRSTW_CPU >>>
17,24  AUX_EN_WOWL >>>
16  WLAN_PCIE_RX_N >>>
16  WLAN_PCIE_RX_P >>>
16  WLAN_PCIE_TX_N >>>
16  WLAN_PCIE_TX_P >>>
16  WLAN_CLK_CPU_N >>>
16  WLAN_CLK_CPU_P >>>
18  WLAN_CLKREQ_CPU_N >>>
18,24  SUS_CLK2  >>>

```



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Reserved			
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Main Func = Power BTN

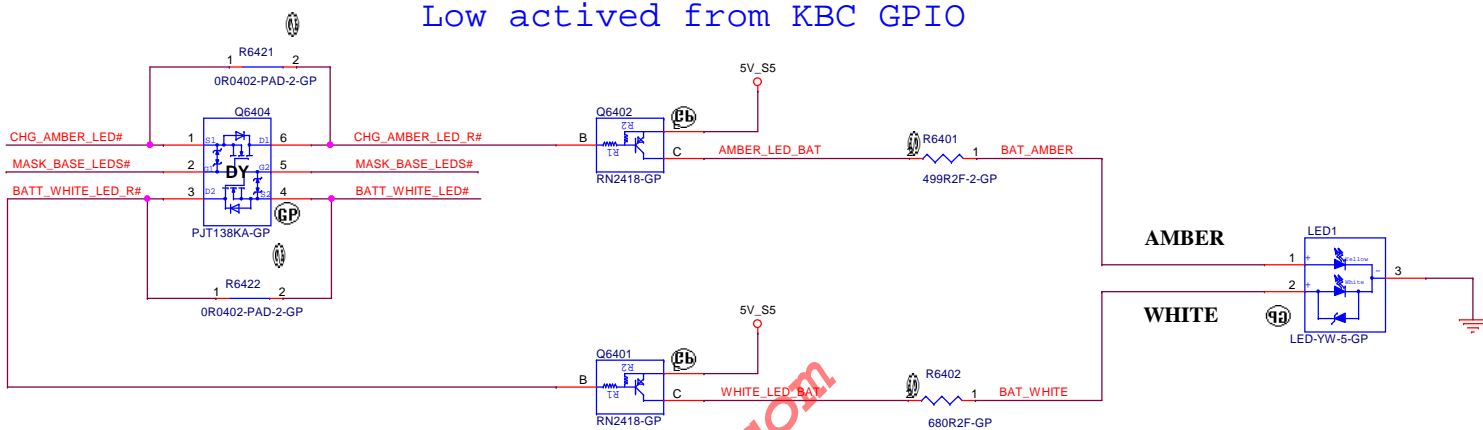
Battery LED1 (AMBER_LED)
Low activated from KBC GPIO

24 CHG_AMBER_LED# >>>—
24 BATT_WHITE_LED# >>>—

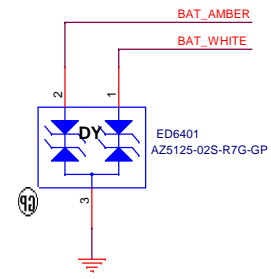
24 SYS_LED_MASK#_R >>>—
16 PCH_SATA_LED# >>>—
63 M2_PCIE_LED# >>>—

24,66,92 LID_CL_SIO# >>>—

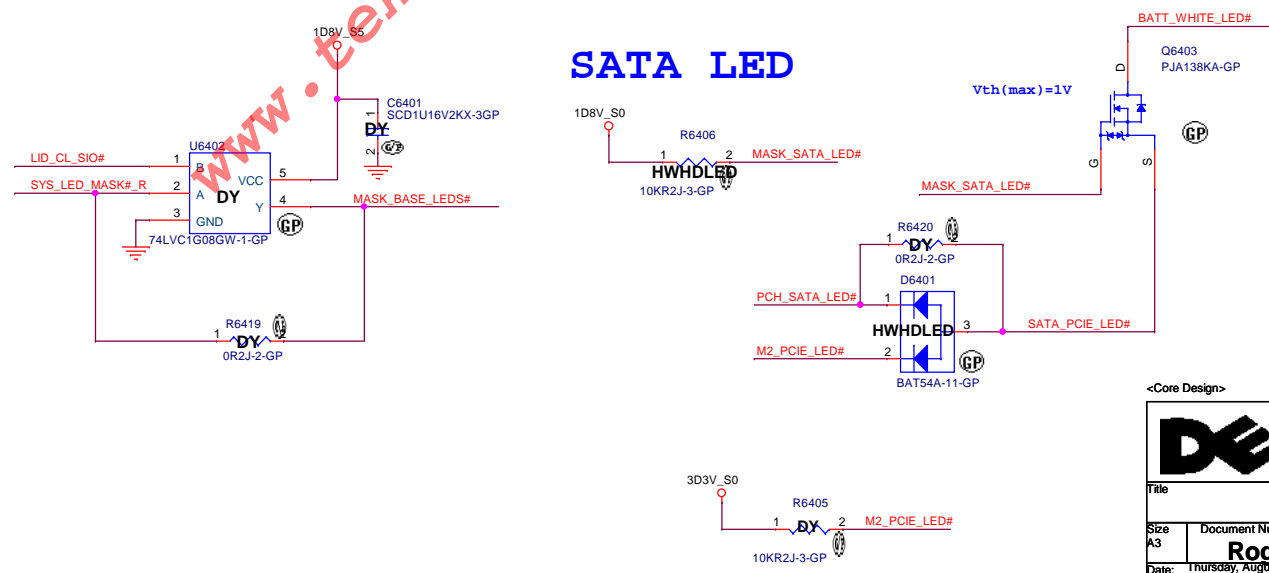
24 MASK_SATA_LED# >>>—



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO



SATA LED



<Core Design>

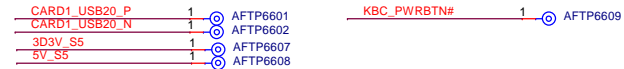
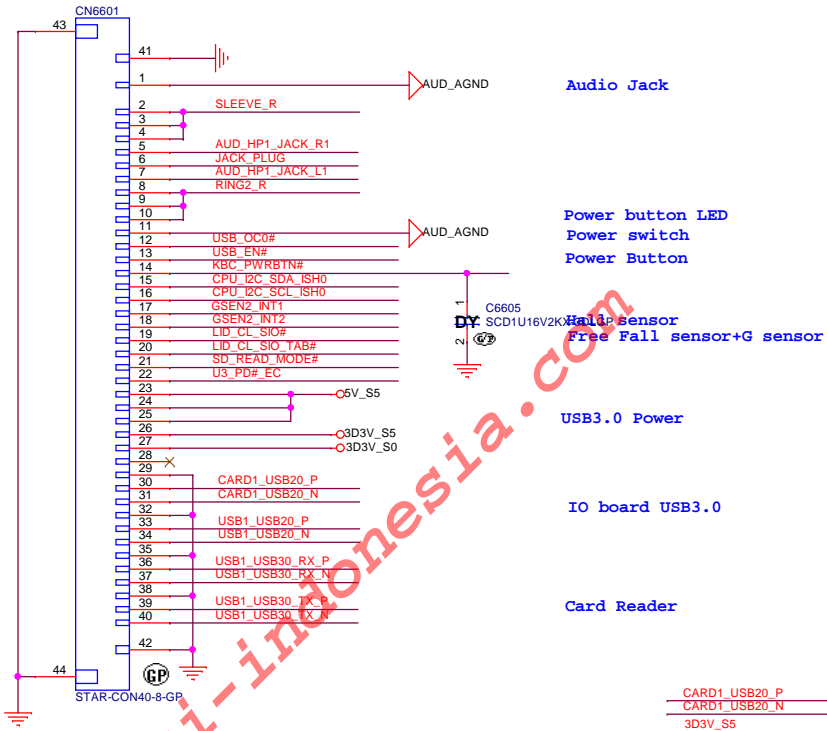
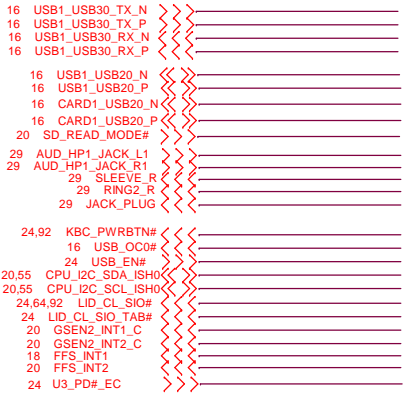
DELL Wistron Corporation
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Title: **LED Board&Power Button**

Size A3 Document Number **SC**

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Main Func = IO Connector



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Size
A4

Document Number

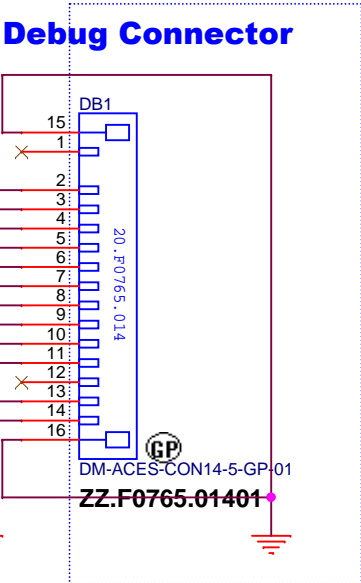
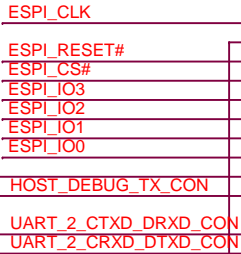
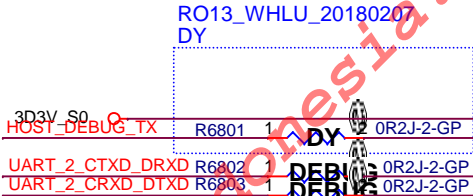
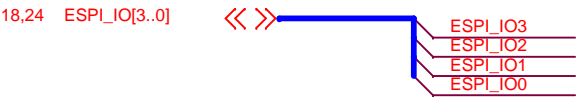
RogueOne 13"

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Main Func = Debug



RO13_20170822
DUMMY PAD to CONNECTOR 20.F0765.014

RO13_A00_20180629
use ZZ.F0765.01401(dummy pad) for MP

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Title

Dubug connector

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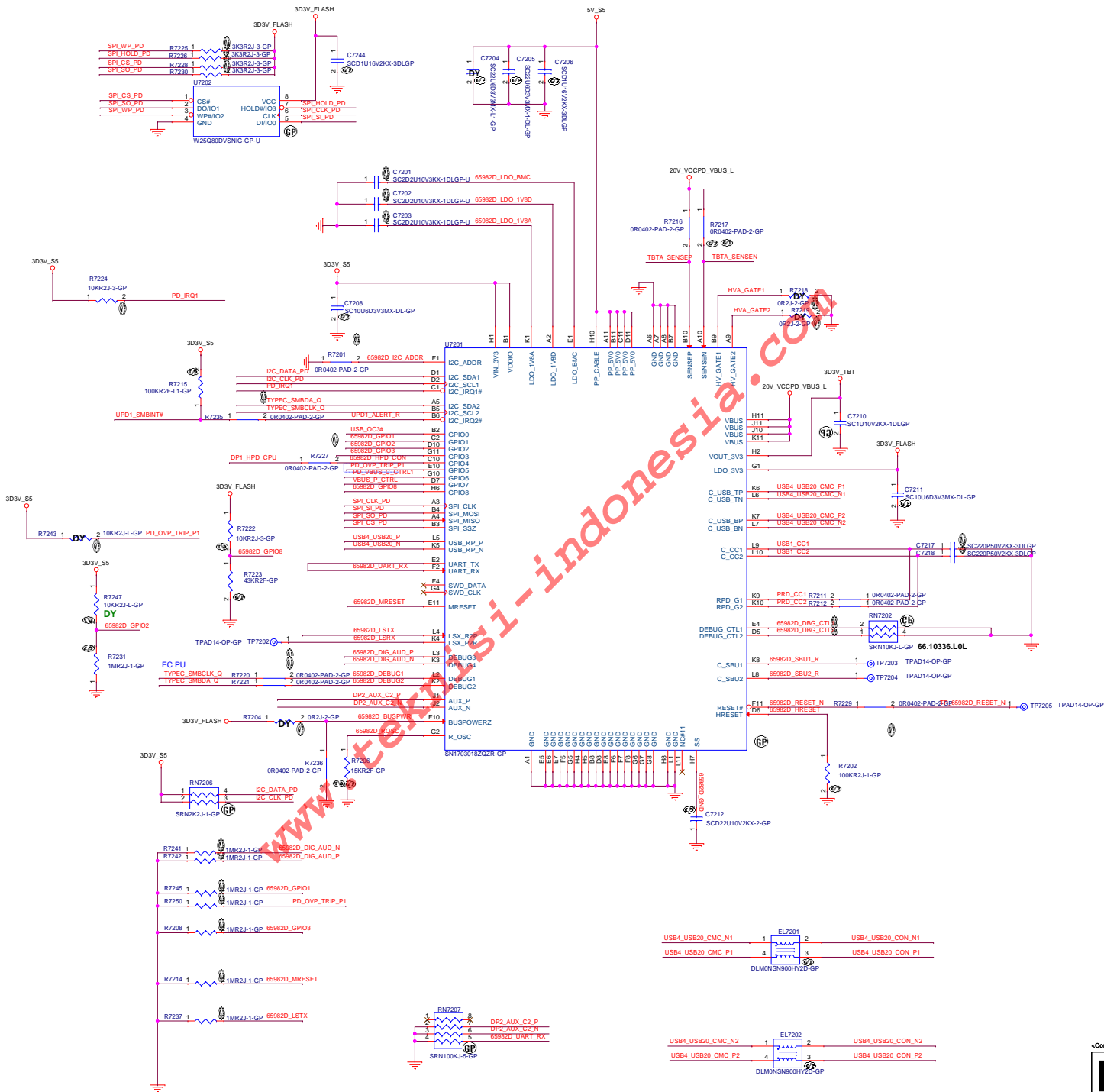
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Main Func = TPS65982DC

- 4,71 DP1_HPD_CU1
74 PD_VBUS_C_CTRL1
16 USB_OC#
71 I2C_CLK_PD
71 I2C_DATA_PD
24 TYPEC_SMBDA_O
24 TYPEC_SMBCLK_O
24 UPD1_SMBINT#
73 USB1_CC1
73 USB1_CC2
73 USB4_USB20_CON_N1
73 USB4_USB20_CON_P1
73 USB4_USB20_CON_N2
73 USB4_USB20_CON_P2
16 USB4_USB20_P
16 USB4_USB20_N



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Main Func = dGPU

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Title			
GPU(5/5)PWR/GND			
Size	Document Number		Rev
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Title		GPU(55)PWR/GND	
Size	Document Number	Rev	
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Title

GPU-VRAM1,2 (1/4)

Size
A3

Document Number
RogueOne 13"

Date: Thursday, August 02, 2018

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SC

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Title RT8812 VGACORE			
Size A2	Document Number RogueOne 13"		Rev SC
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Title

GPU-VRAM7,8 (4/4)

Size
A3

Document Number
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Title

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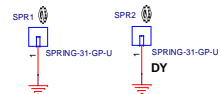
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Document Number
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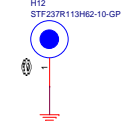
Rev
SC

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34.4YW18.001

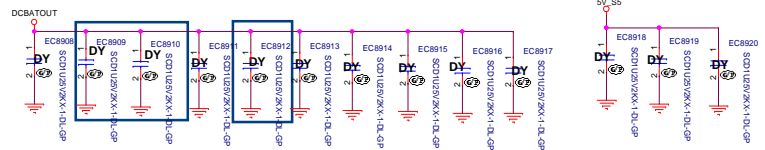


Type-C

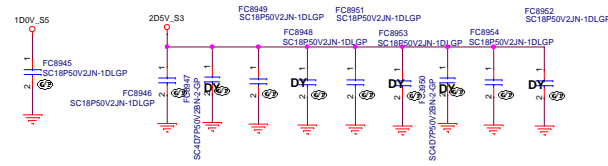
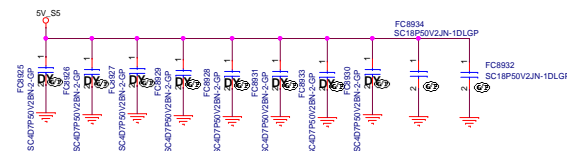
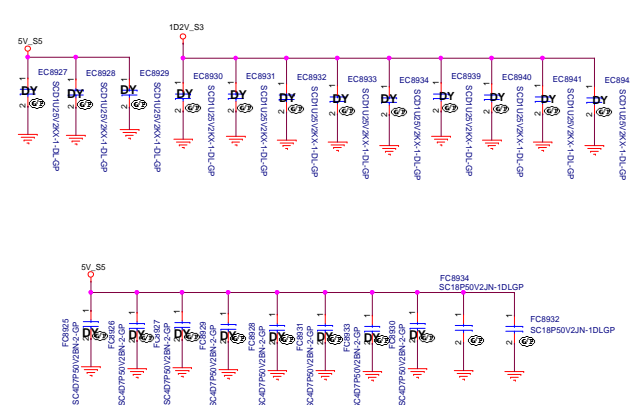
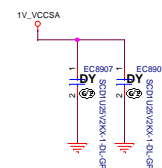
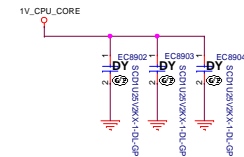
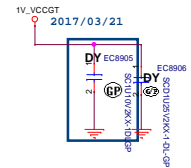
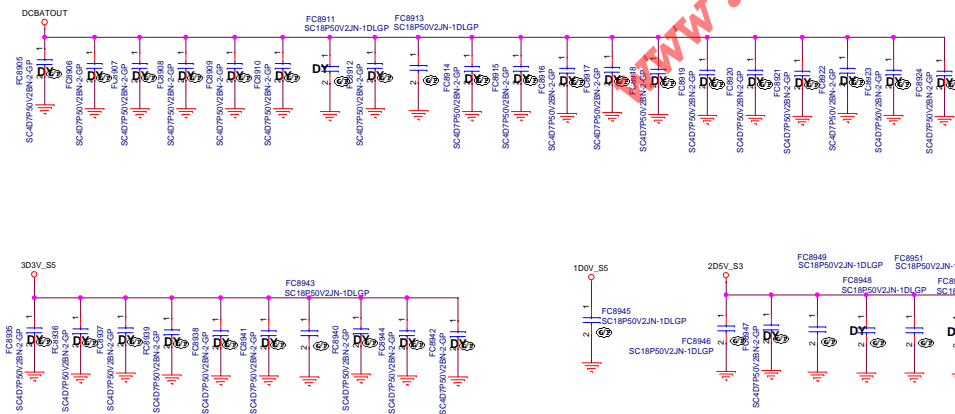


SSID = EMI

Mind the voltage rating of the caps.



SSID = RF



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Title			UNUSED PARTS/EMI Capacitors
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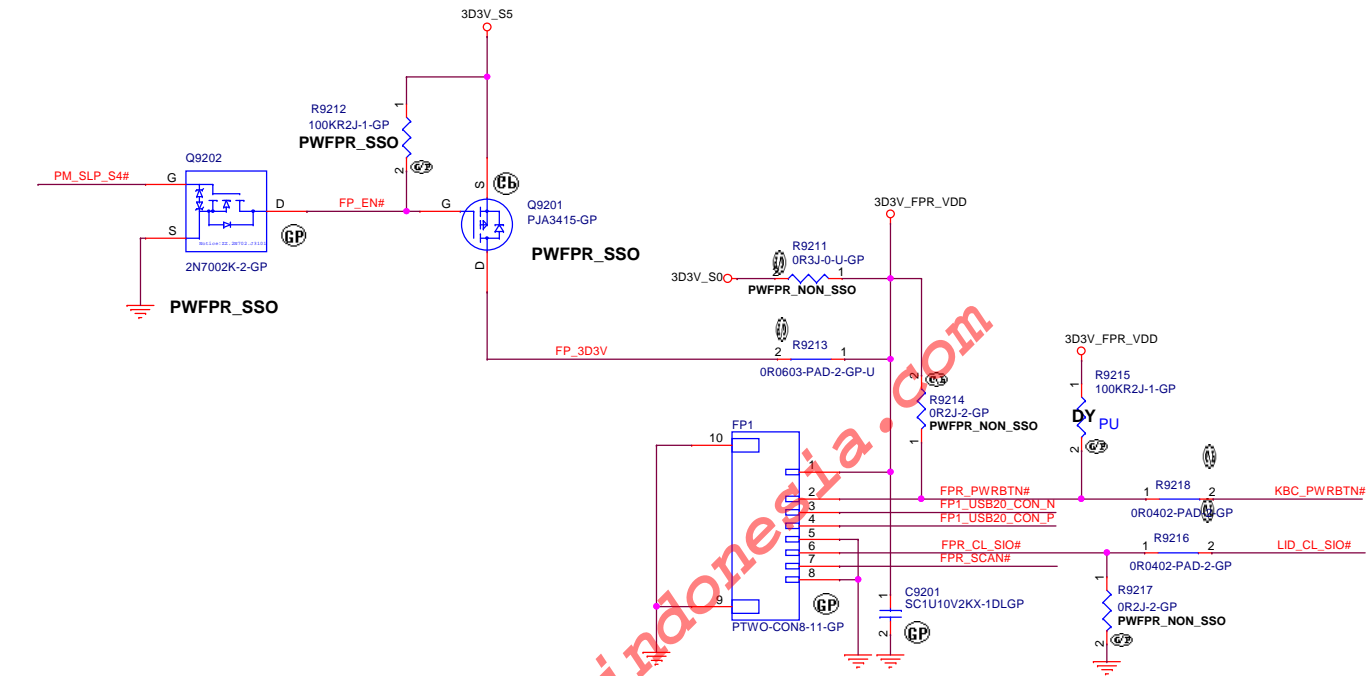
Size	Document Number	Rev
A3	RogueOne 13"	SC

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Main Func = FPR

- 16 FP1_USB20_N <<>>
- 16 FP1_USB20_P <<>>
- 24 FPR_SCAN# >>>
- 17,40,54 PM_SLP_S4# >>>
- 24,66 KBC_PWRBTN# >>>
- 24,64,66 LID_CL_SIO# >>>

FBR(Botton side finger Print Sensor)

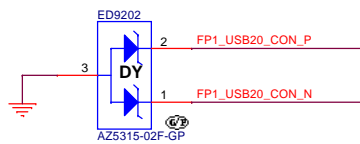
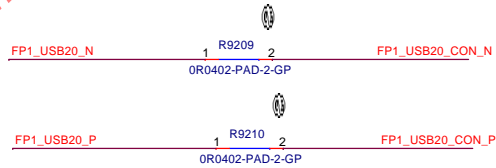


	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

GF5288WN1+GF128A+GM168 Module design

Pin Definition

CN PIN MAP	
PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPT0_key shielding
8	GND(ID pin)



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Title: (Reserved)Finger Print

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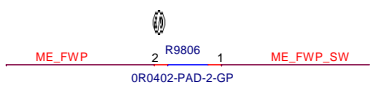
Sheet 95 of 106

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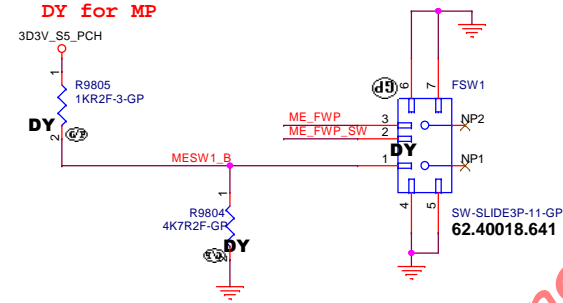
Main Func = SWITCH

24 ME_FWP >>>
19 ME_FWP_SW <<<



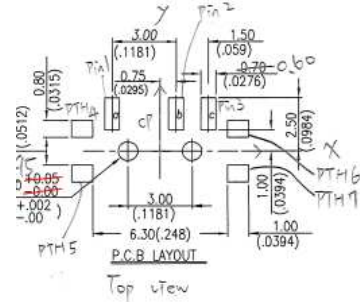
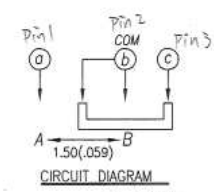
Firmware SW

Default setting:pull LOW
DY for MP



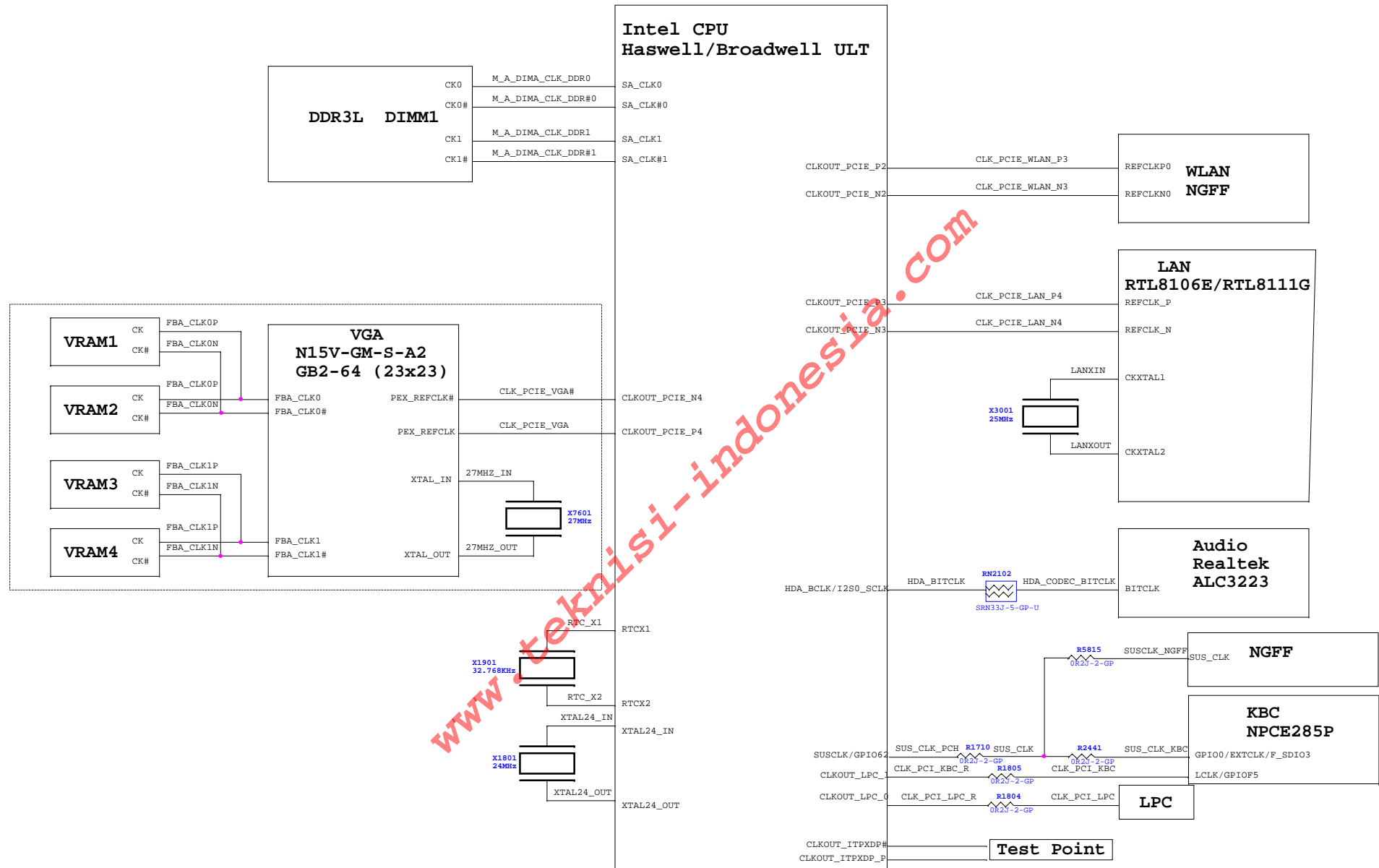
	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

*Symbol same as
62.40018.641



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CLK Block Diagram



[illegible]

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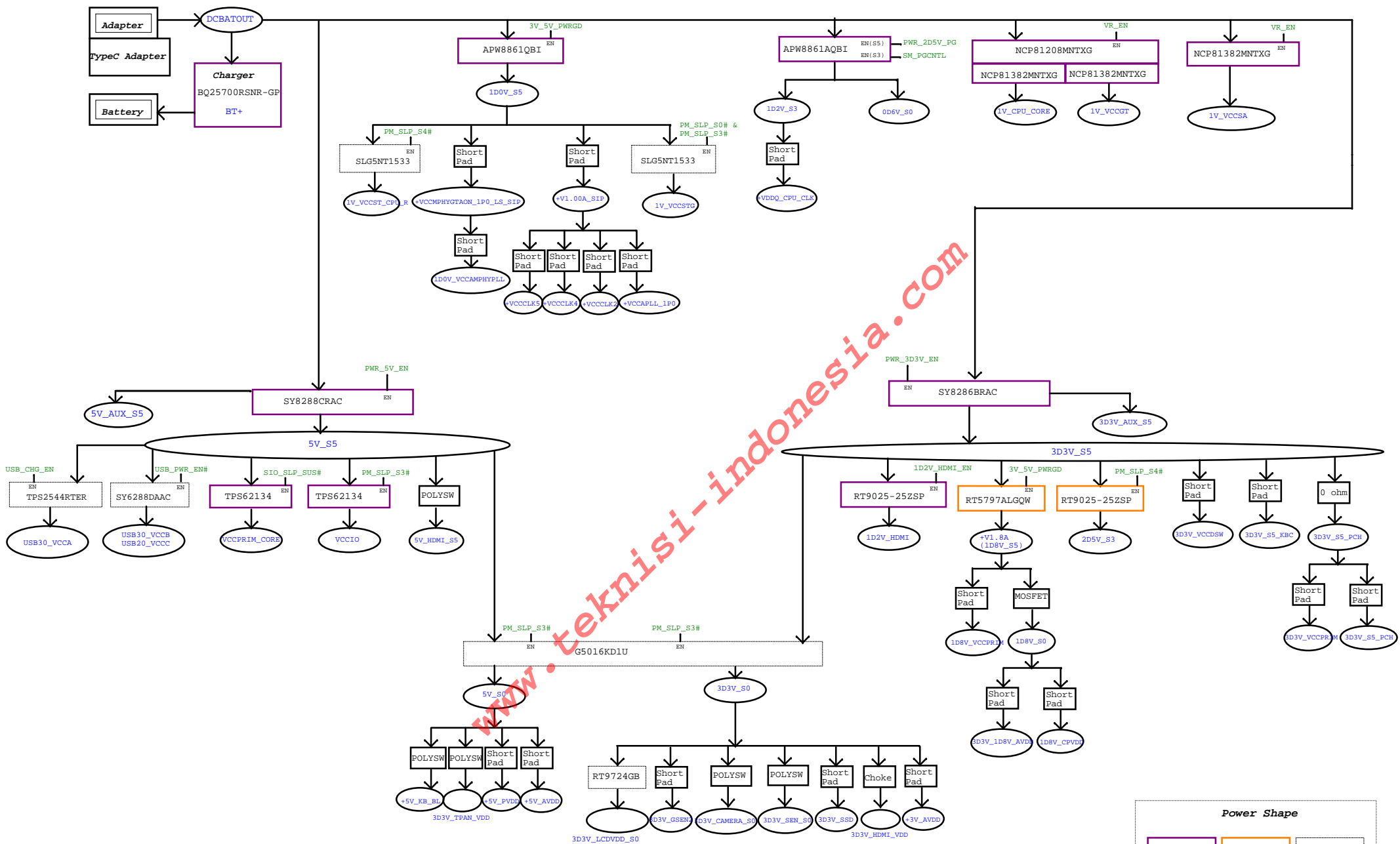
The diagram illustrates the timing relationships for various signals in the i.MX6Q processor. Key signals include VttVto, RTYSTR, Vt0S0L3, DSW_P0R0K, B0T0DR, SLP_S0R0, SLP_P0R0_S0R0, PCH Pin/M0py Rate, RSM0S70, S0PWR0NACK, S0S0SLP, AC0P0M0NT, S0S0_A0K0, PWR0S70, SLP_A0, P0t0m0 V0u0A0W, SLP_A0R0, V0u0_L0A0R0Y, SLP_R0L0A0, V0u0_L0A0, SLP_S0R0, SLP_A0, SLP_S0W, SLP_0W, E0P0_R0S0T0, CL_A0P0, V0E0S7_V0u0P0L, V0E0S70, V0P0, V0DQ_V0u0P0_0C, V0C0D0, V0C0S0, V7T, D0P0_V7T_C0V0L, V0DQ_P0R0000, M0P_V0R0A0D0, P0W0R_V7T_R0L0, A0L_S0S0_P0R000, V0C0E7_P0R000, PCH_P0R0K, PCH C0M0 O0u0b, P0R0C0R0000, M0P_V0R0_0, C0P_S0D_B0S, SLP_P0R0K, S0L_P0R0, P0L7R0P, V0C0, V0C0E7, T0E0M0T0R0W, S0P_S0S0, and D0R_R0S0E70. The diagram shows the timing relationships between these signals, including setup and hold times, and is annotated with 'Note 1' and 'Note 2'.

Timing diagram showing the relationship between 2D5V_S3, 1D2V_S3, and 0D6V_S0 signals. The signals are shown as digital waveforms. 2D5V_S3 and 1D2V_S3 are high for most of the duration, while 0D6V_S0 is low for most of the duration. There are transitions in all three signals at approximately 1/3 and 2/3 of the time period.

The diagram illustrates the power and control circuitry for a Kabylake-U MCP. Key components and their connections include:

- Power Input:** A 3.7V battery connected to a BQ25504 charger IC, which is then connected to a 3.3V regulator (RT5797ALQW) and a 3.0V regulator (RT9025-2525B).
- Control and Timing:** An RTC (DS1307) is connected to the system. A KBC (MEC1416) is used for keyboard control, connected to the MCP's KBC pins.
- Memory and Storage:** An A02262QI memory IC is connected to the MCP's memory pins. A TP622961 is connected to the MCP's TP622961 pin.
- Other ICs:** An AP22966 is connected to the MCP's AP22966 pin. A TP622913B is connected to the MCP's TP622913B pin. A TP622961 is connected to the MCP's TP622961 pin.
- Level Shifter:** A Level Shifter (74VHC125) is used to interface the MCP's CPU SVID pins with the SA/Clare/OT pins.
- Annotations:** The diagram includes several text annotations, such as "RT5797ALQW: Delay 10 ms after reset", "RT9025-2525B: Delay 10ms after reset", and "TP622961: Delay 10ms after reset".

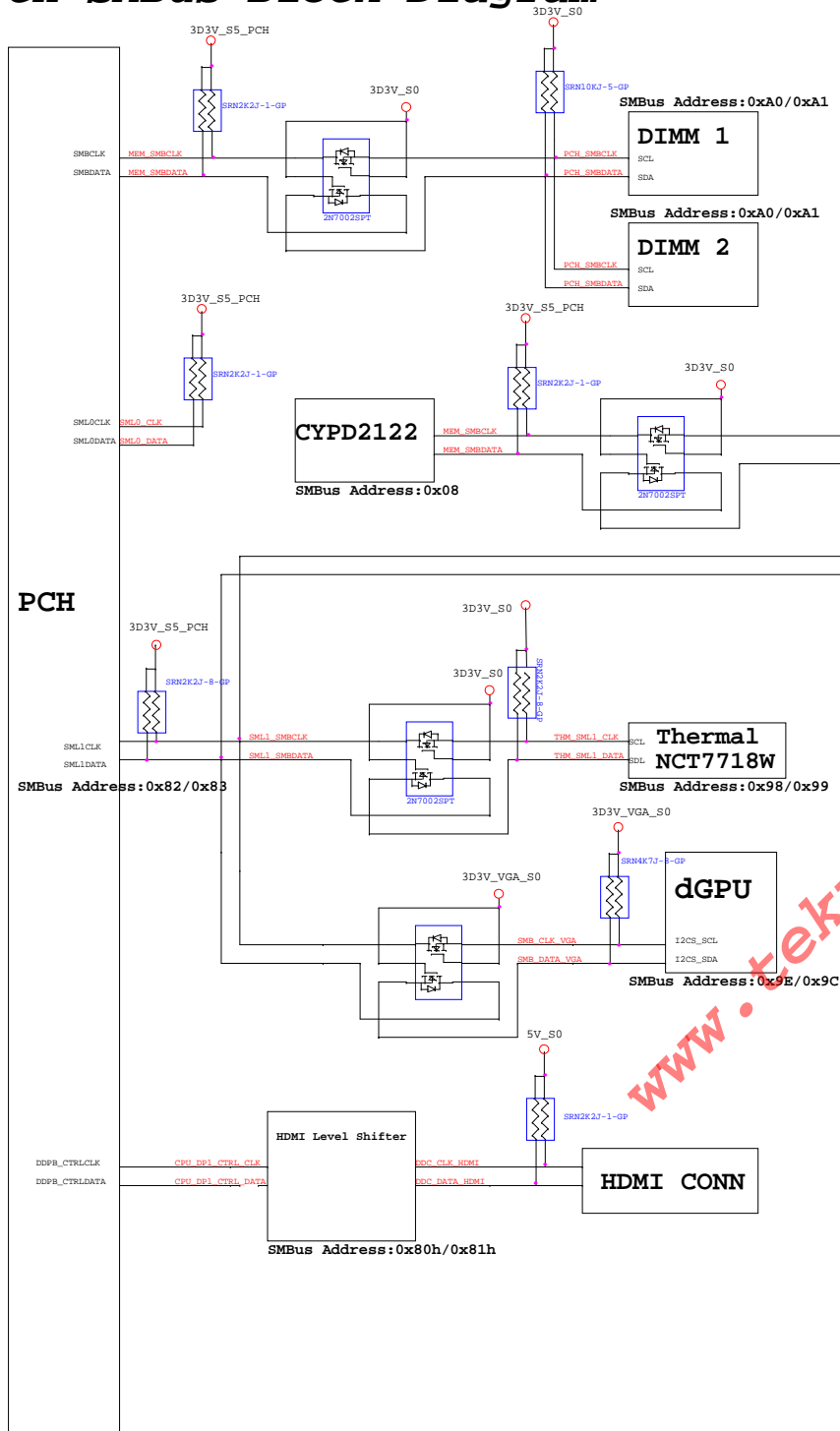
At the bottom of the page, there is a row of 35 numbered circles (1-35) corresponding to the callouts in the diagram.



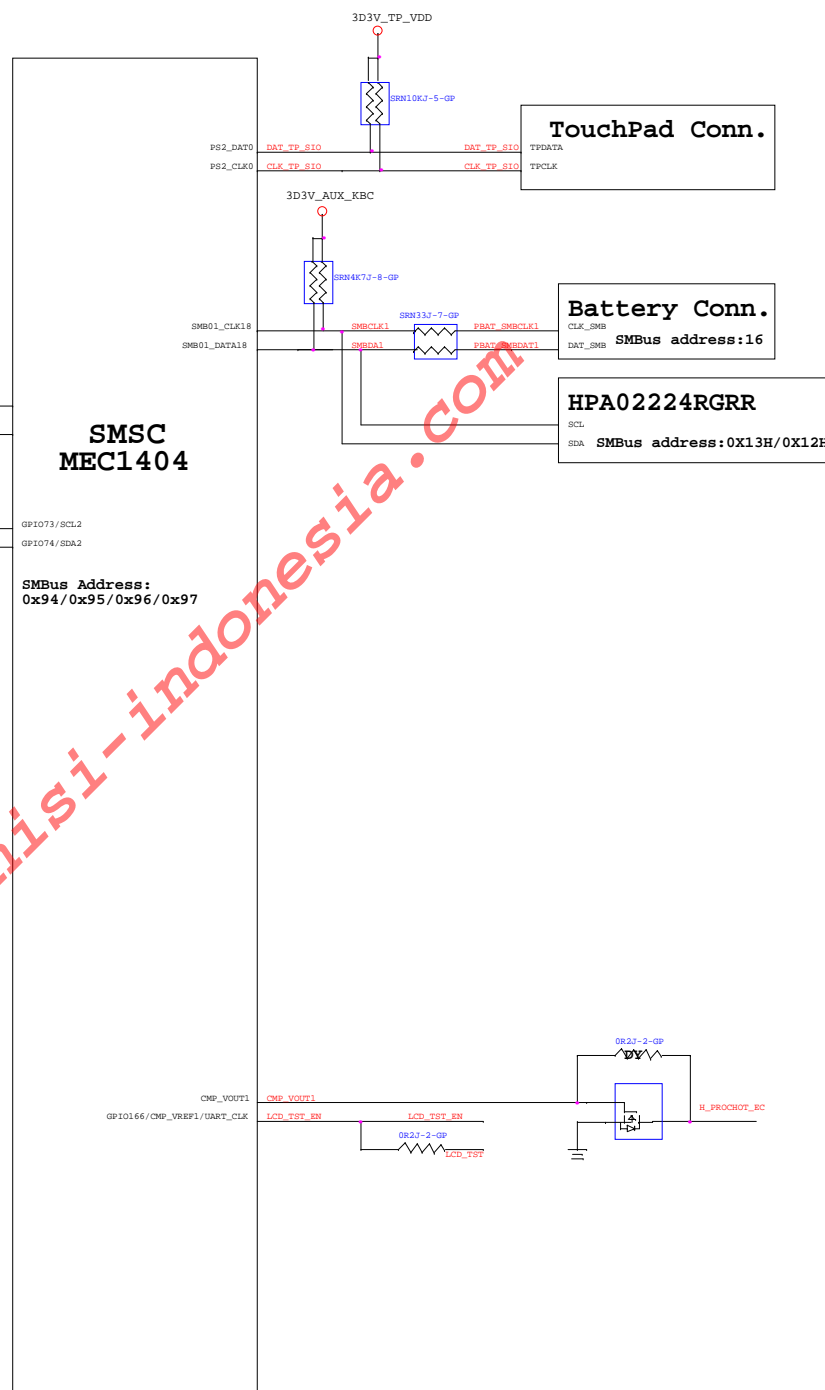
Power Shape

Regulator	LDO	Switch
-----------	-----	--------

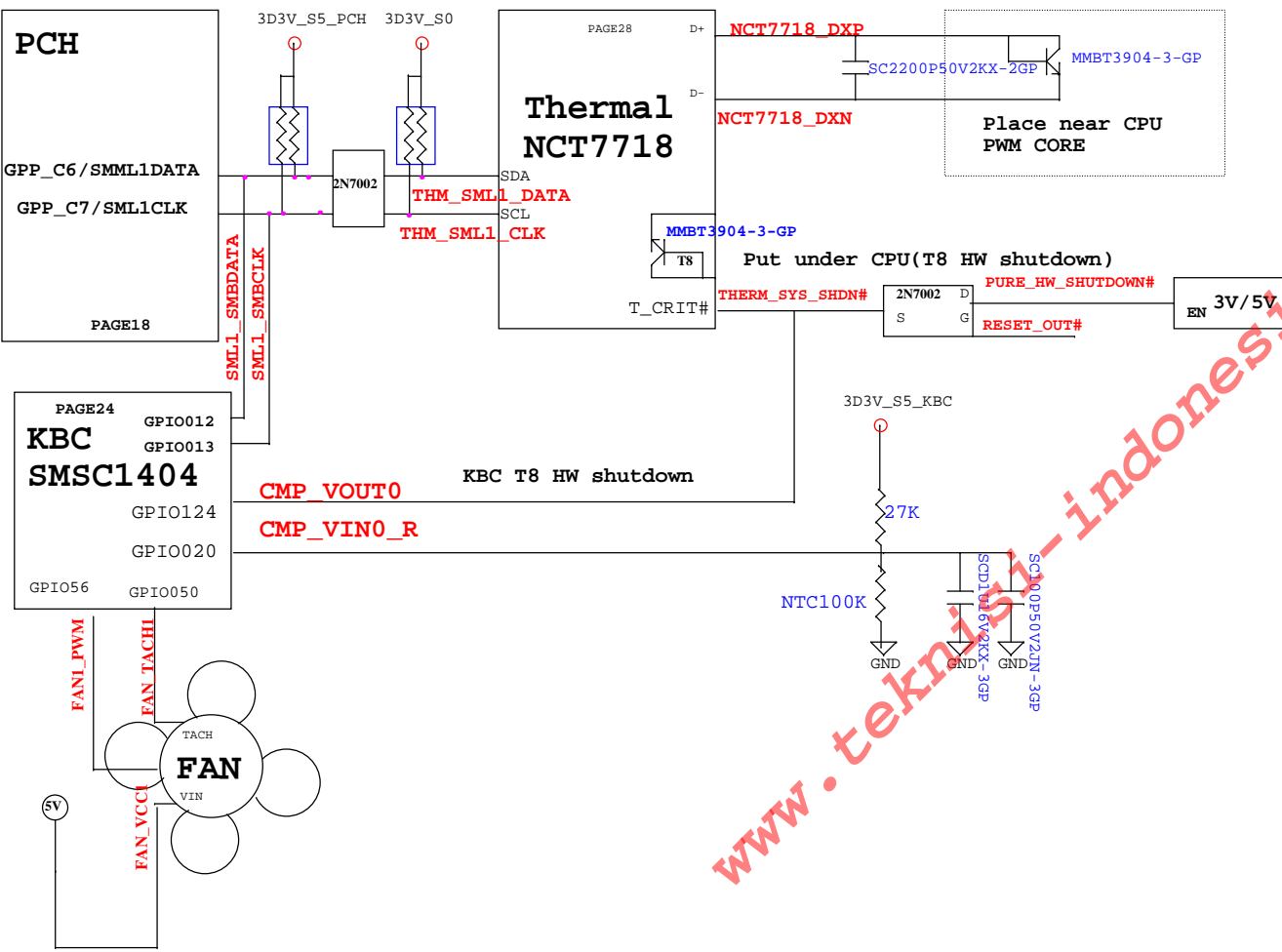
PCH SMBus Block Diagram



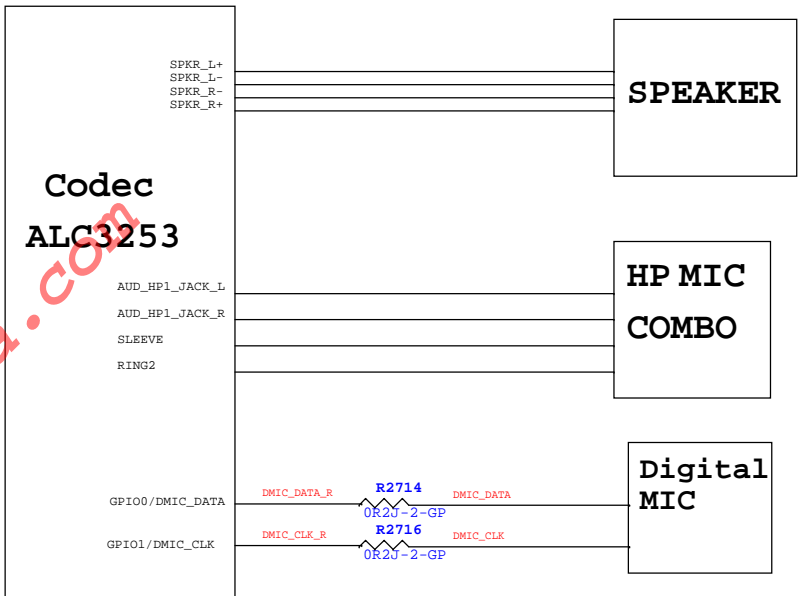
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Title

SIP connector

Size
A

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